

# Compal confidential

## Schematics Document

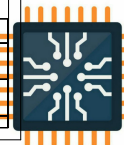
Mobile Arrandale rPGA989 with  
Intel PCH (Ibex Peak-M) core logic

2009-11-05

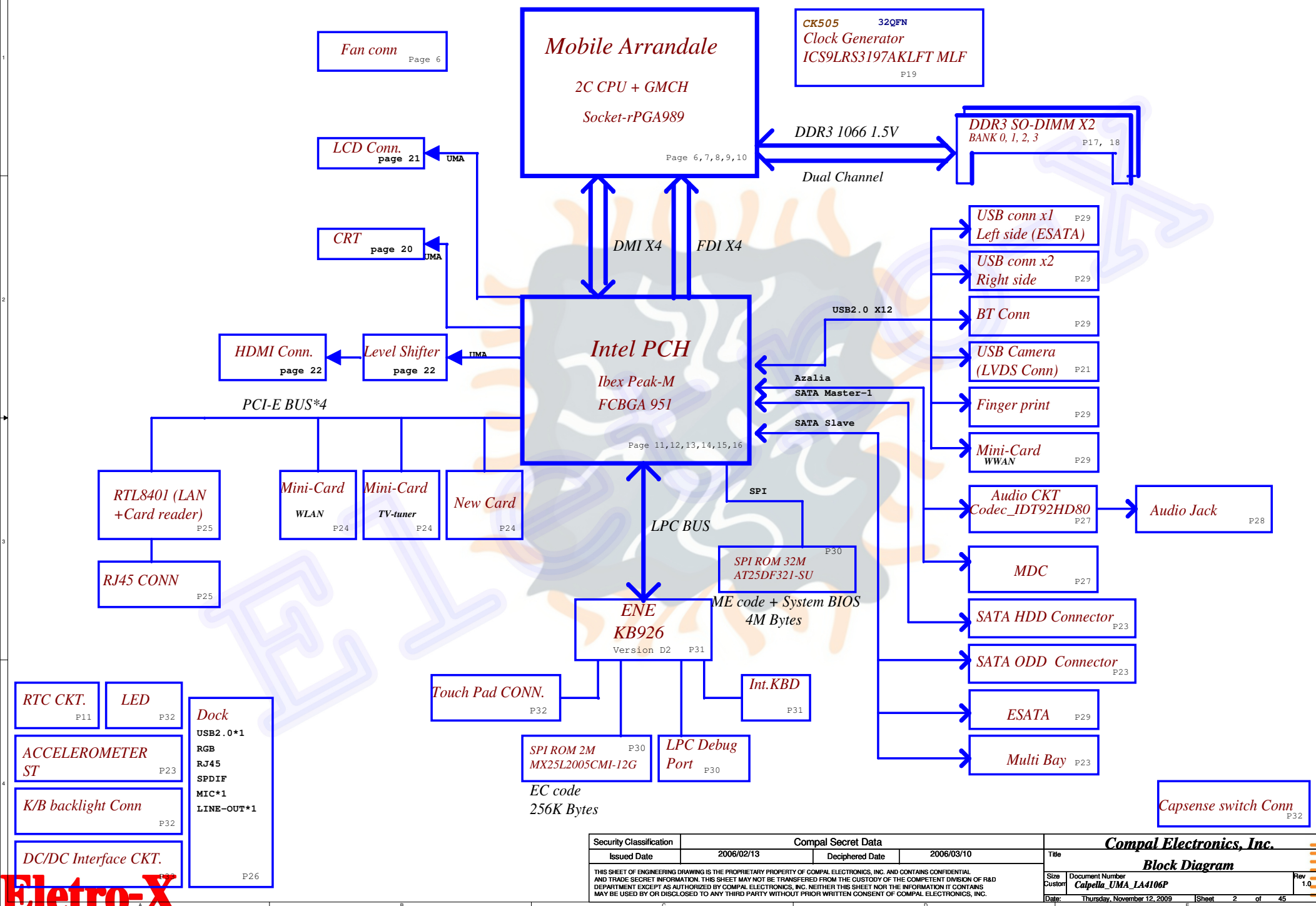
REV 1.0

機 等 密	硬體二部	
	產出人員	
	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	Cover Sheet	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	Calpella_UMA_LA4106P	1.0
				Date:	Thursday, November 12, 2009	Sheet 1 of 45







Security Classification		Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date	2006/03/10
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.			
Block Diagram			
Size	Document Number	Rev	1.0
Custor	Calpella_UMA_LA4106P		
Date	Thursday, November 12, 2009	Sheet	2 of 45



O MEANS ON

X MEANS OFF

power plane State	+B VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.05VS +1.5VS_CPU
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**: means Analog Ground**

**45@ :** means need be mounted when 45 level assy or rework stage.

**CONN@ : means ME part**

**OPP@ : For POWER BUTTON (NO CAP SERSOR)**

**DEBUG@ : For DEBUG**



USB-0	Left side(with ESATA)
USB-1	Right side
USB-2	Right side
USB-3	Dock
USB-4	Camera
USB-5	MiniCard(WLAN)
USB-6	X (HM55 don't support)
USB-7	X (HM55 don't support)
USB-8	MiniCard(WWAN)
USB-9	New Card
USB-10	X
USB-11	Finger Printer
USB-12	Bluetooth
USB-13	X

PCle-1	WWAN
PCle-2	WLAN
PCle-3	RTL8401 Combo
PCle-4	New card
PCle-5	X
PCle-6	X
PCle-7	X (HM55 don't support)
PCle-8	X (HM55 don't support)

SATA0	HDD
SATA1	ODD
SATA2	X (HM55 don't support)
SATA3	X (HM55 don't support)
SATA4	ESATA
SATA5	Multi Bay

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK GEN	WWAN	WLAN	M93 Thermal Sensor	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	X	X	X	V	V	V	V	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
VCCP		+3VS			+3VS	+3VS	+3VS @+3VAL W	+3VS @+3VALW	+3VL		+3VS	+3VS

+3VL

+3VALW

+3VS/+3VALW

+3VALW

**CONNECTED**

ZZZ

DAZ0BI00100  
PA@

ZZZ

DAZ0BI00400

OPP@

PCB: DA60000F400  
PA@: DAZ0BI00600 (w/o SIM daughter/B)  
OPP@: DAZ0BI00400

DEVICE	HEX	ADDRESS
--------	-----	---------

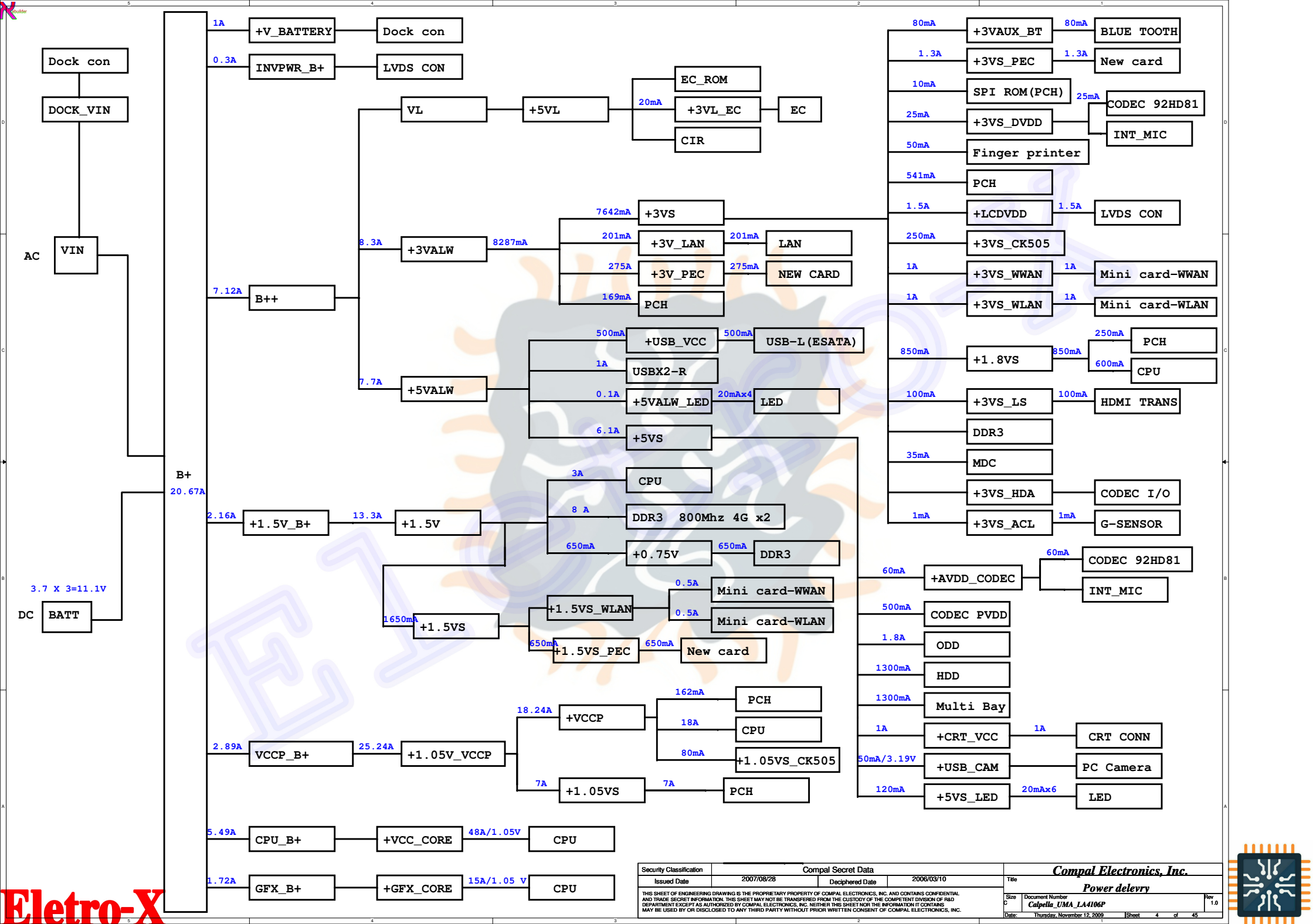
DDR SO-DIMM0	A0	10100000
DDR SO-DIMM1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
G sensor	1D	00011101

DEVICE	HEX	ADDRESS
--------	-----	---------

Smart Battery  
Cap Sensor board

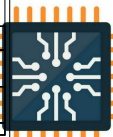




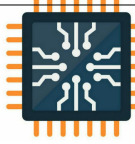
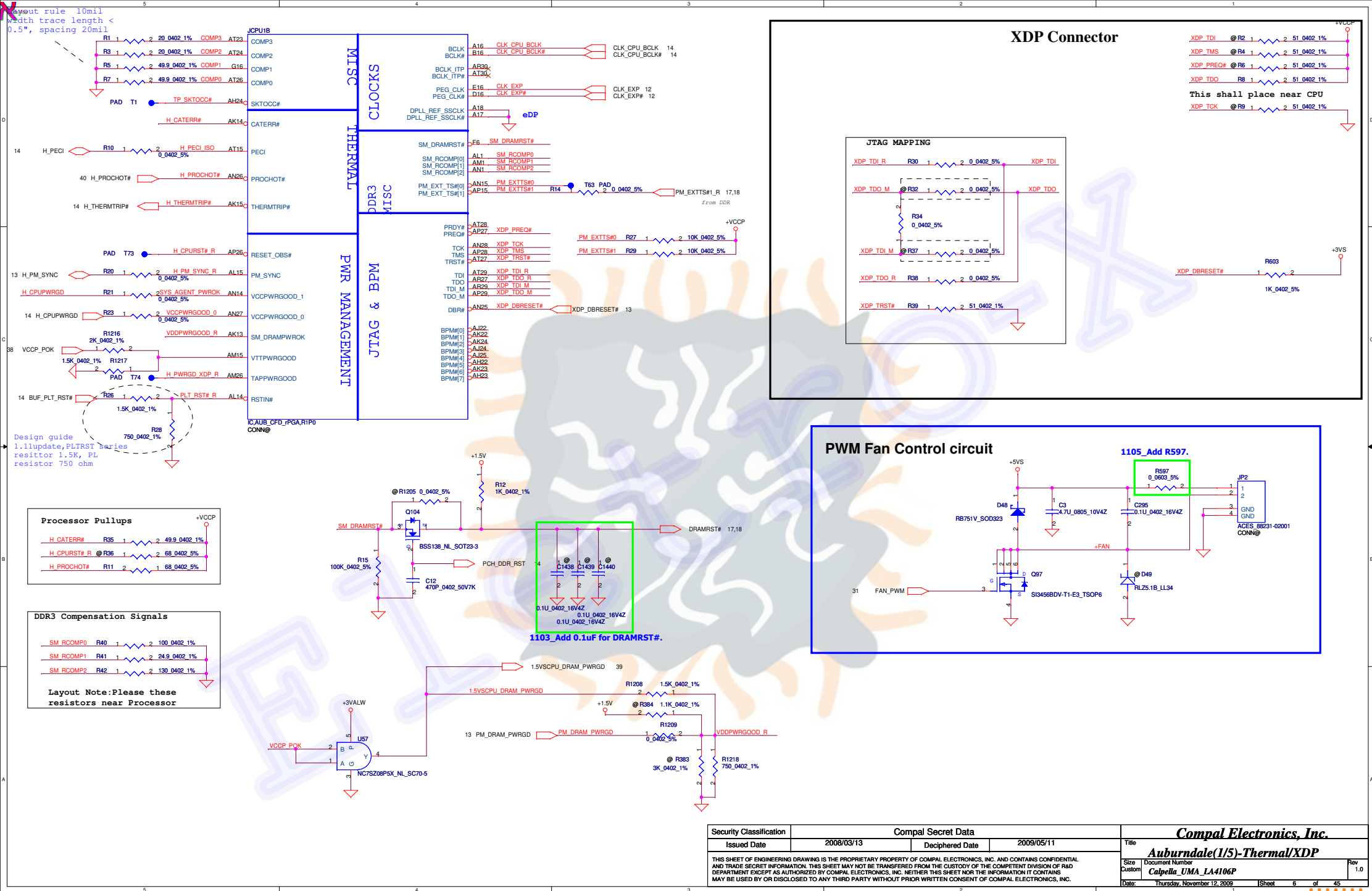




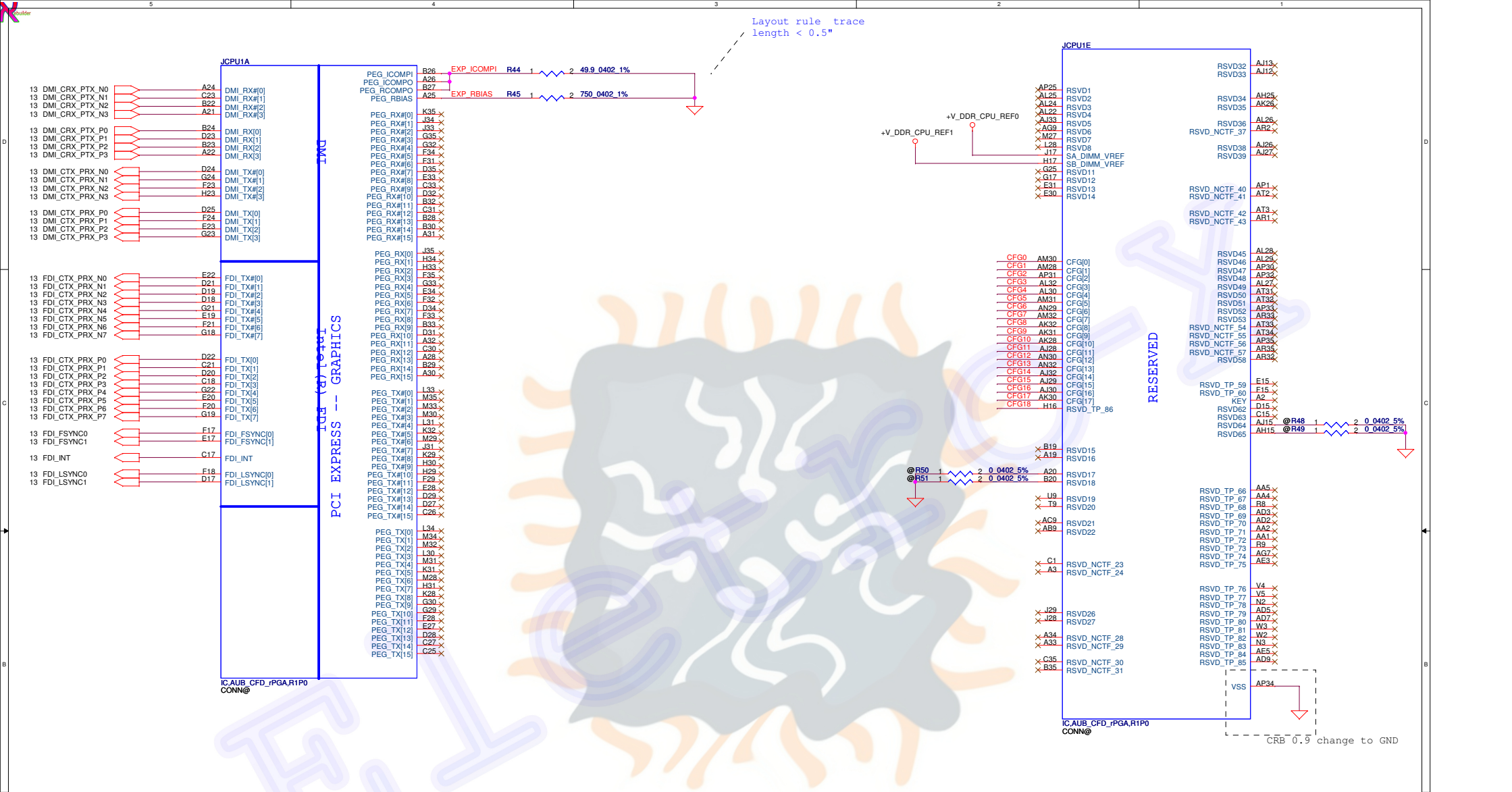
## Max











## CFG Straps for PROCESSOR

CFG0 @R52 1 2 3.01K 0402 1%

PCI-Express Configuration Select

CFG0

1: Single PEG  
0: Bifurcation enabled

Not applicable for Embedded Processor

CFG3 R54 1 2 3.01K 0402 1%

CFG3-PCI Express Static Lane Reversal

CFG3

1: Normal Operation  
0: Lane Numbers Reversed  
15 -> 0, 14 -> 1, .... \*

CFG4 @R53 1 2 3.01K 0402 1%

CFG4-Display Port Presence

CFG4

1: Disabled; No Physical Display Port  
0: Enabled; An external device is connected to the Embedded Display Port

CFG7 @R55 1 2 3.01K 0402 1%

Only temporary for early CFD samples (rPGA/BGA)  
Only for pre ES1 sample

CFG7 @R55 PD 3.01K on CFG7 for PCIe Jitter  
MW33 don't staff

Security Classification		Compal Secret Data		Title	
Issued Date	2008/03/13	Deciphered Date	2009/05/11	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	Calpella_UMA_LA4106P
Date	Thursday, November 12, 2009	Sheet	7 of 45	Rev	1.0

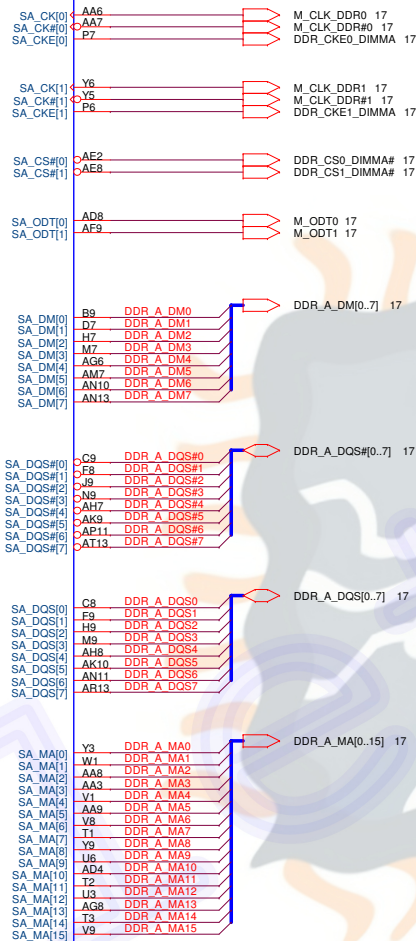




JCPU1C

IC,AUB\_CFD\_rPGA,R1P0  
CONN@

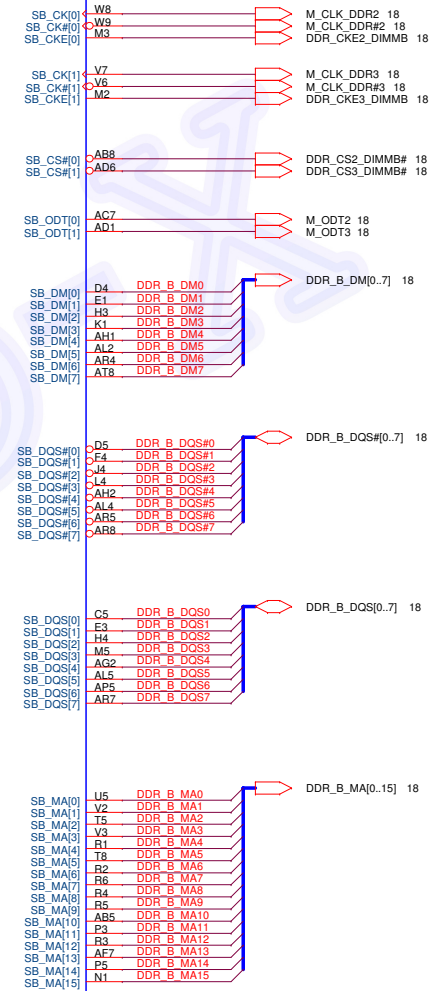
DDR SYSTEM MEMORY A



JCPU1D

IC,AUB\_CFD\_rPGA,R1P0  
CONN@

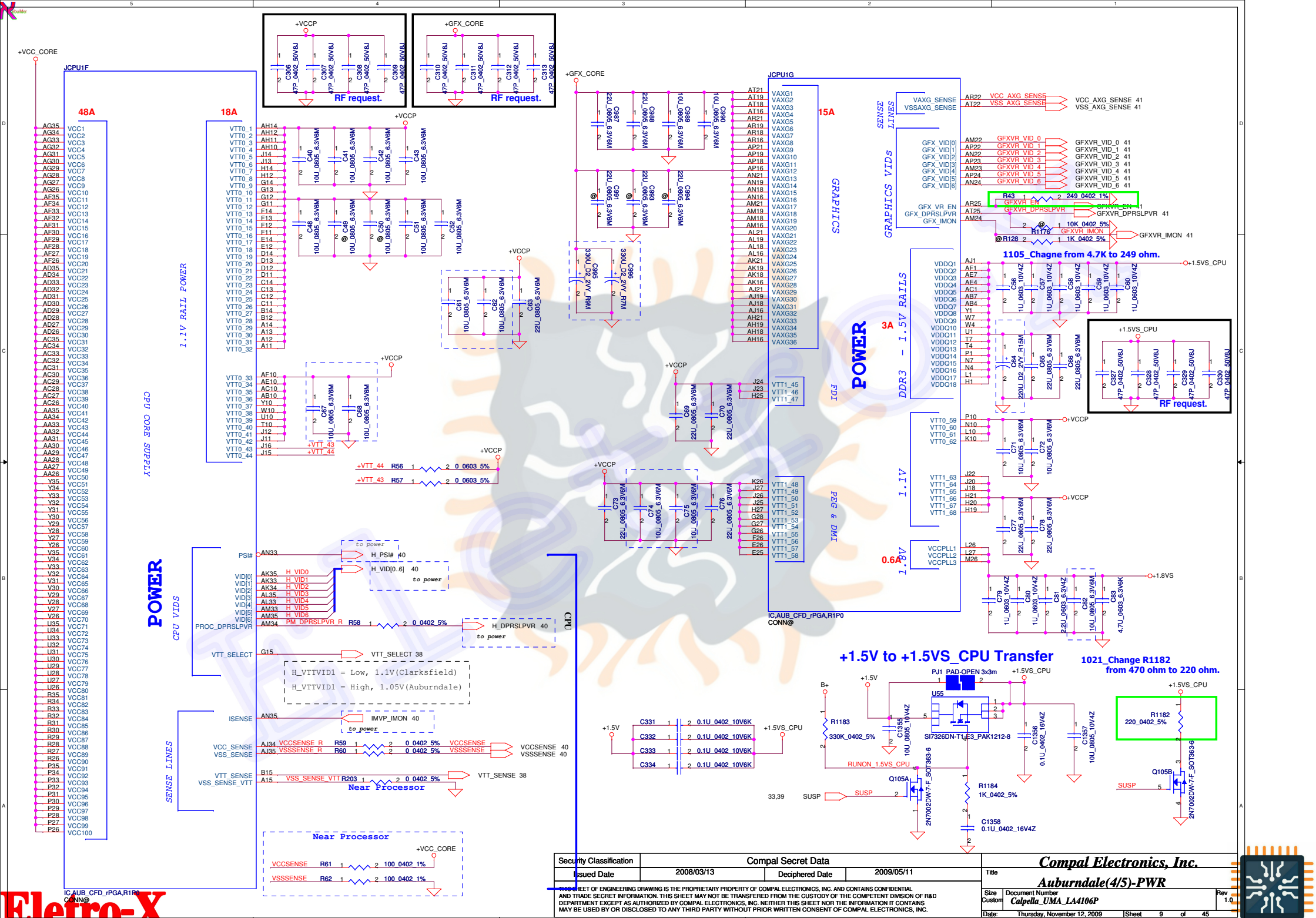
DDR SYSTEM MEMORY - B



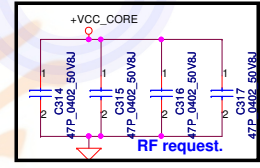
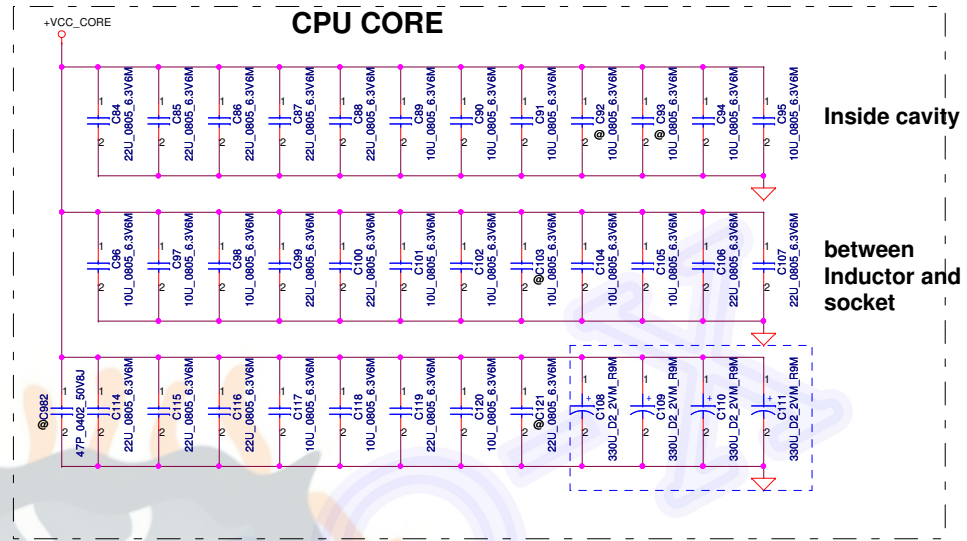
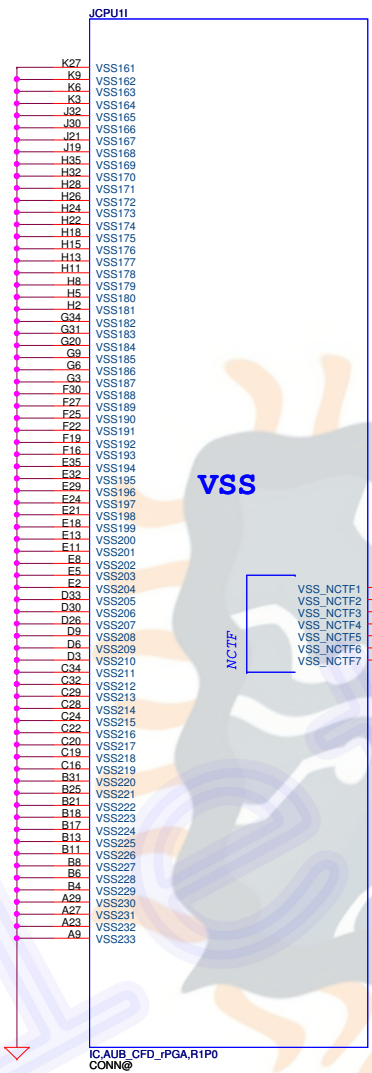
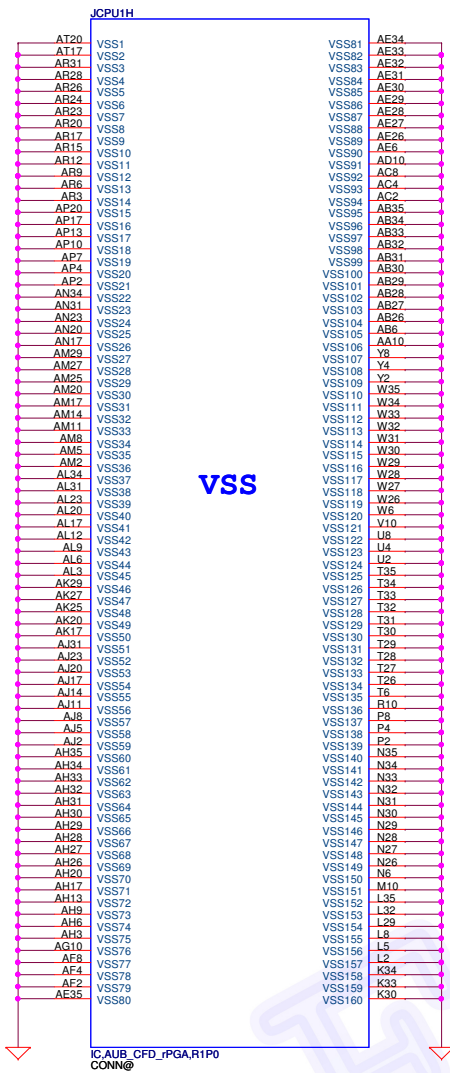
Security Classification			Compal Secret Data		Title	
Issued Date	2008/03/13	Deciphered Date	2009/05/11		Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	Calpella_UMA_LA4106P	1.0
				Date	Thursday, November 12, 2009	Sheet 8 of 45



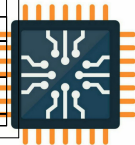




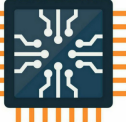




Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2008/03/13		Deciphered Date		2009/05/11		Title			
								Auburndale(5/5)-GND/Bypass			
								Size			
								Document Number			
								Calpella_UMA_LA4106P			
								Date			
								Thursday, November 12, 2009			
								Sheet			
								10 of 45			









WWAN

WLAN

LAN+Cardreader

New Card

WWAN

WLAN

LAN+Card reader

New Card

New Card

New Card

New Card

New Card

New Card

New Card

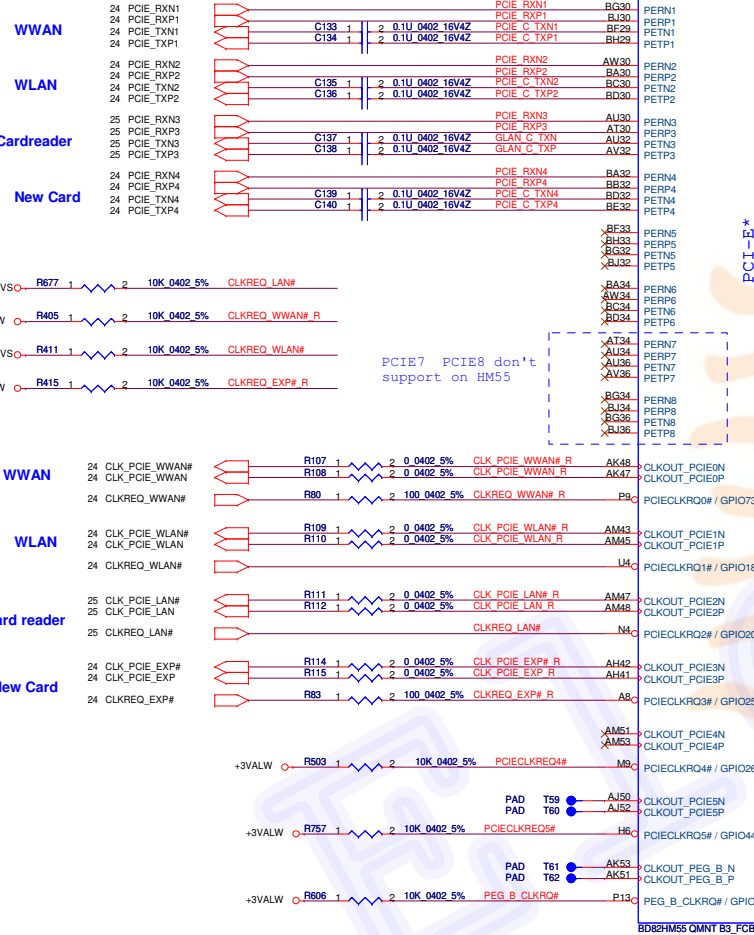
New Card

New Card

New Card

New Card

New Card



UIB

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PCI-E\*

PERN1

PERN2

PERN3

PERN4

PERN5

PERN6

PERN7

PERN8

PERN9

PERN10

PERN11

PERN12

PERN13

PERN14

PERN15

PERN16

PERN17

PERN18

PERN19

PERN20

PERN21

PERN22

PERN23

PERN24

PERN25

PERN26

PERN27

PERN28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

PERP5

PERP6

PERP7

PERP8

PERP9

PERP10

PERP11

PERP12

PERP13

PERP14

PERP15

PERP16

PERP17

PERP18

PERP19

PERP20

PERP21

PERP22

PERP23

PERP24

PERP25

PERP26

PERP27

PERP28

PERP1

PERP2

PERP3

PERP4

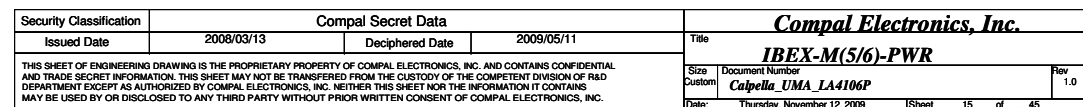




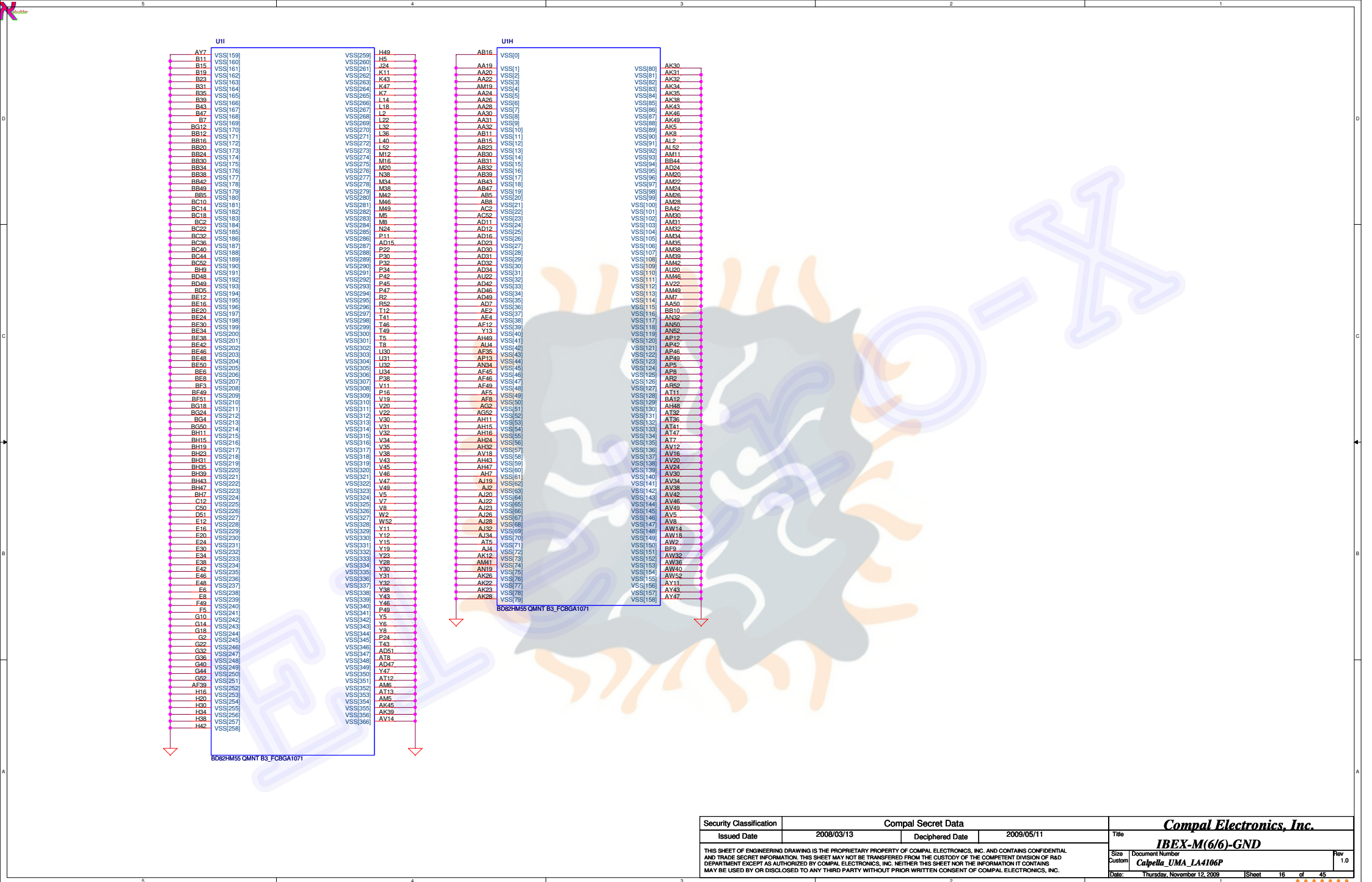




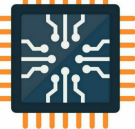




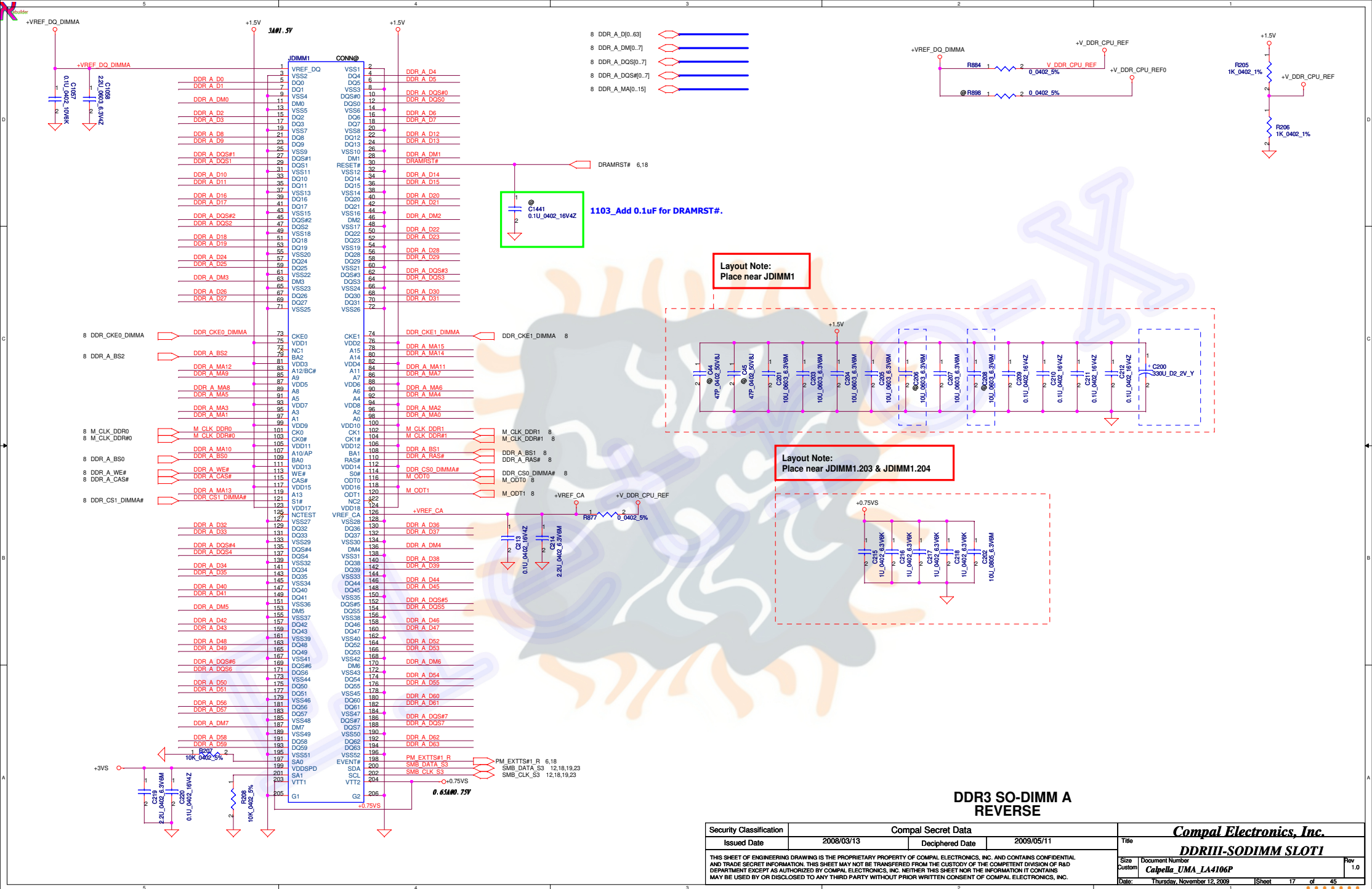




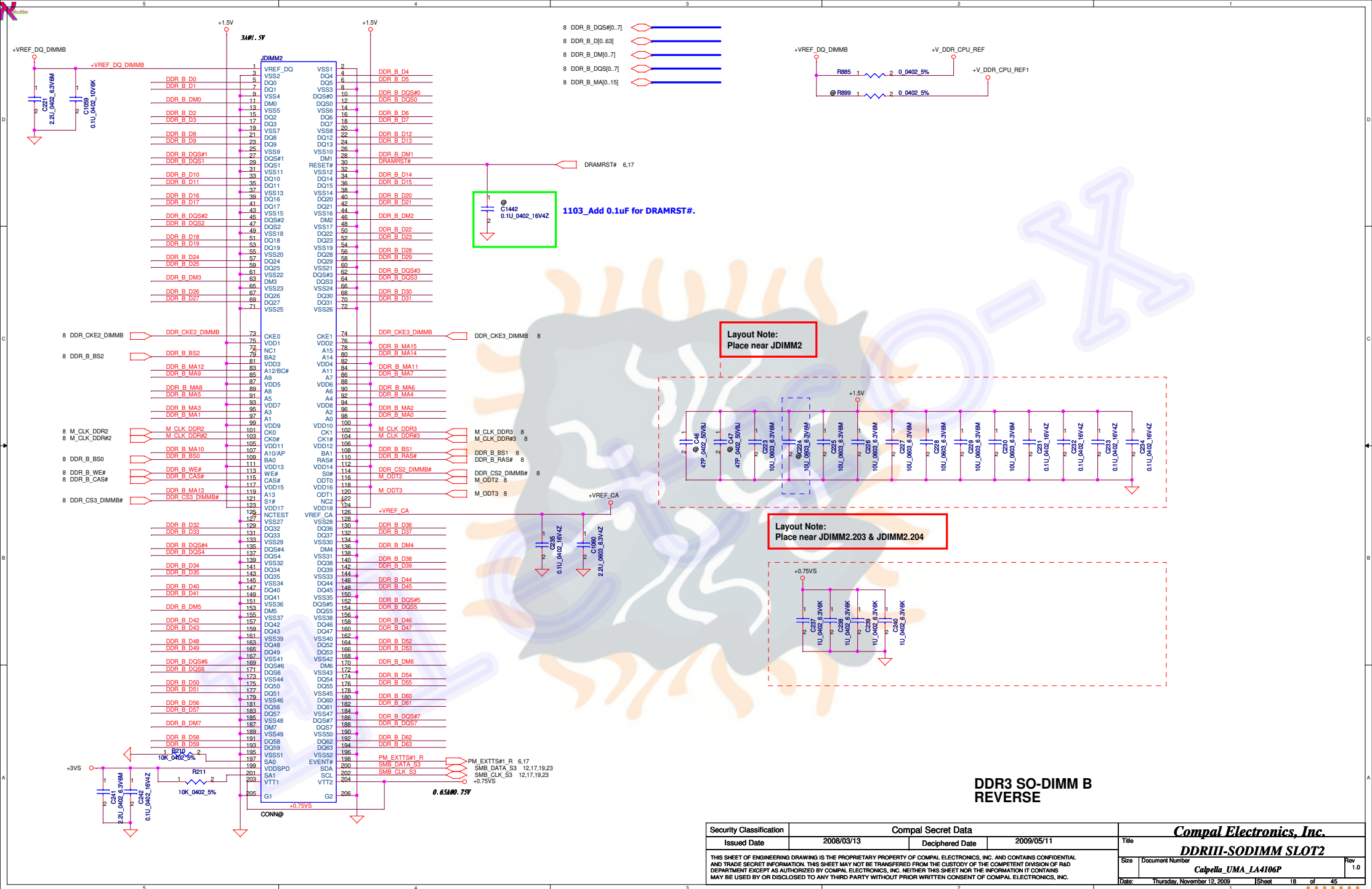
Security Classification		Compal Secret Data		Title	
Issued Date	2008/03/13	Deciphered Date	2009/05/11	IBEX-M(6/6)-GND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 1.0
Date: Thursday, November 12, 2009		ISheet 16		of 45	









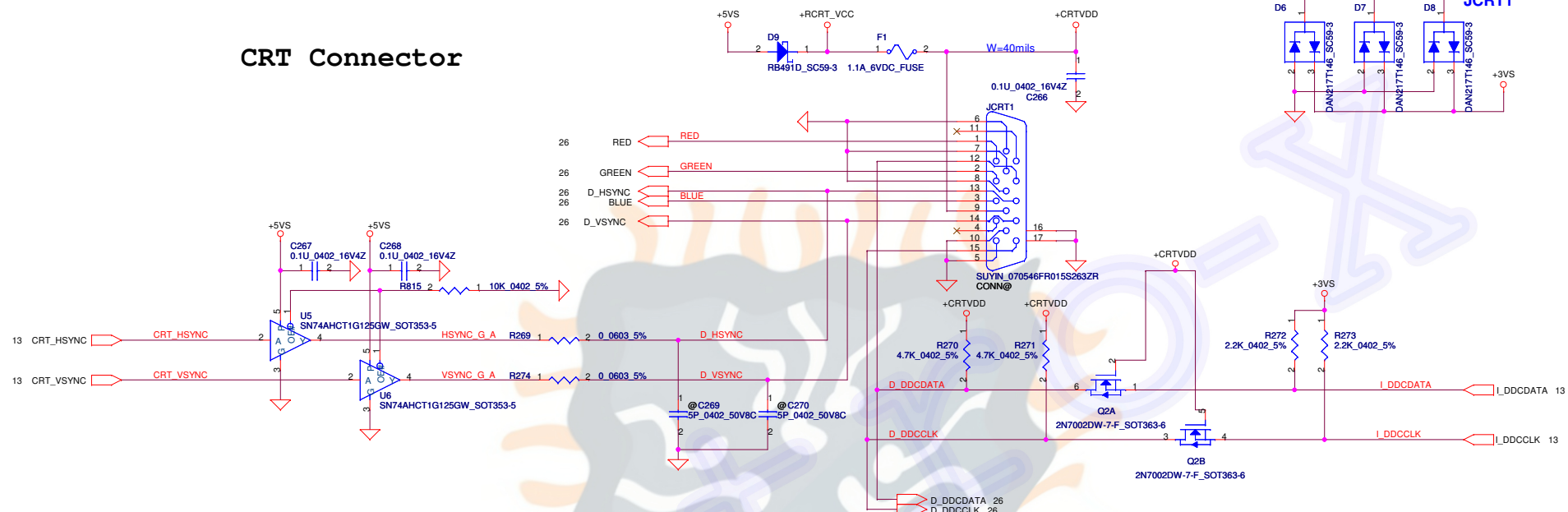




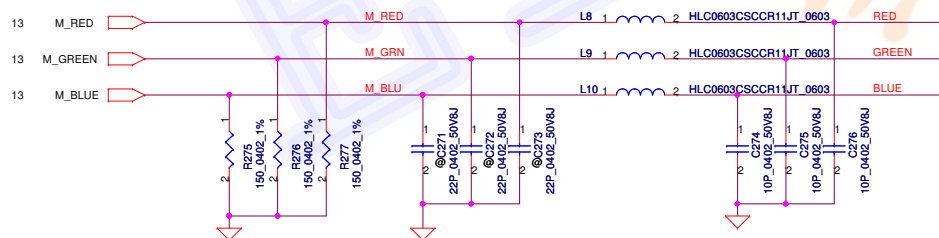




## CRT Connector



## CRT Termination/EMI Filter



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Rev	1.0
				Calpella_UMA_LA4106P	
				Date:	Thursday, November 12, 2009
				Sheet	20 of 45





# Eletro-X



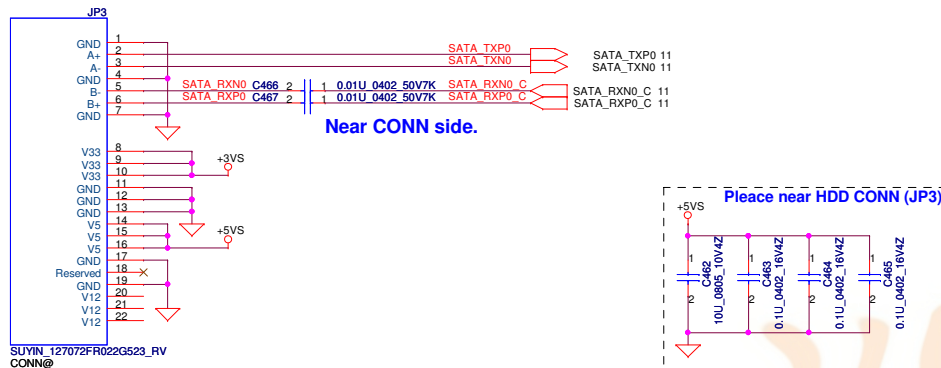
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>					
Issued Date		2007/08/28	Deciphered Date		2006/07/26	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						<b>LCD CONN.</b>			
						Size	Document Number		Rev
						Capella_UMA_LA4106P			1.
						Date:	Thursday, November 12, 2009		Sheet 21 of 45



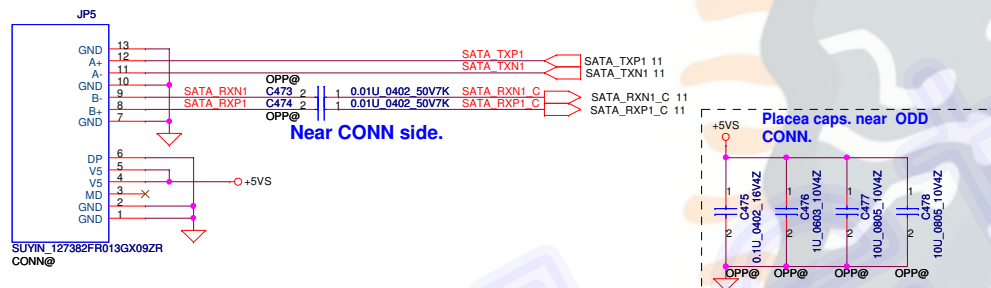




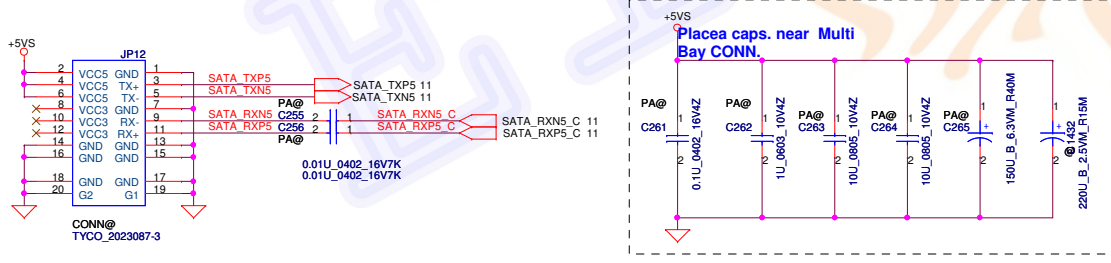
## HDD Connector



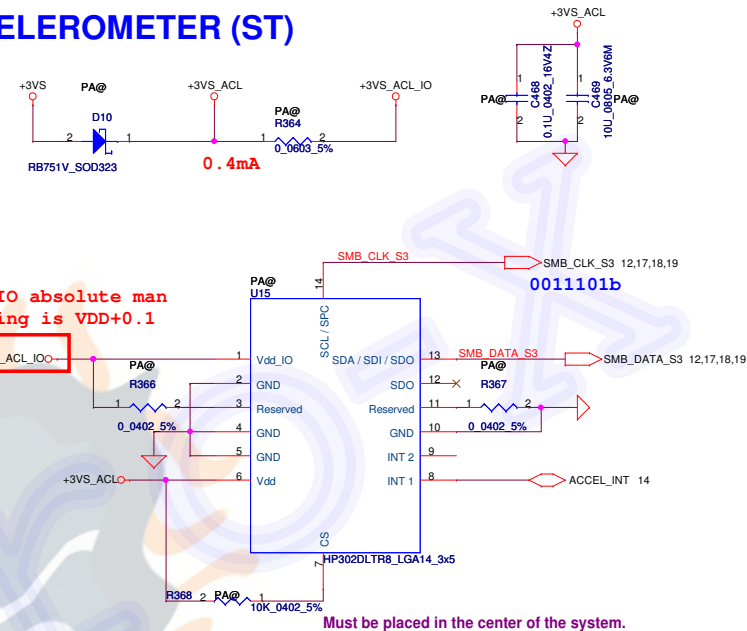
## CD-ROM Connector



## Multi Bay



## ACCELEROMETER (ST)



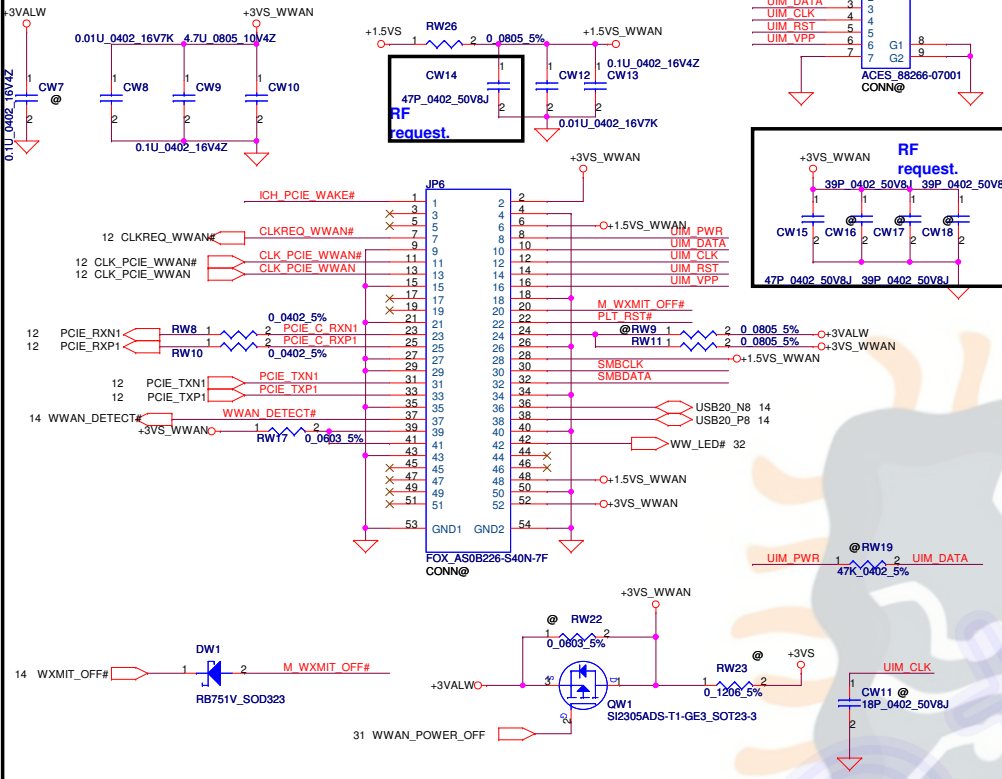
Security Classification	Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom
				Calpella_UMA_LA4106P
				Rev 1.0
				Date: Thursday, November 12, 2009
				Sheet 23 of 45



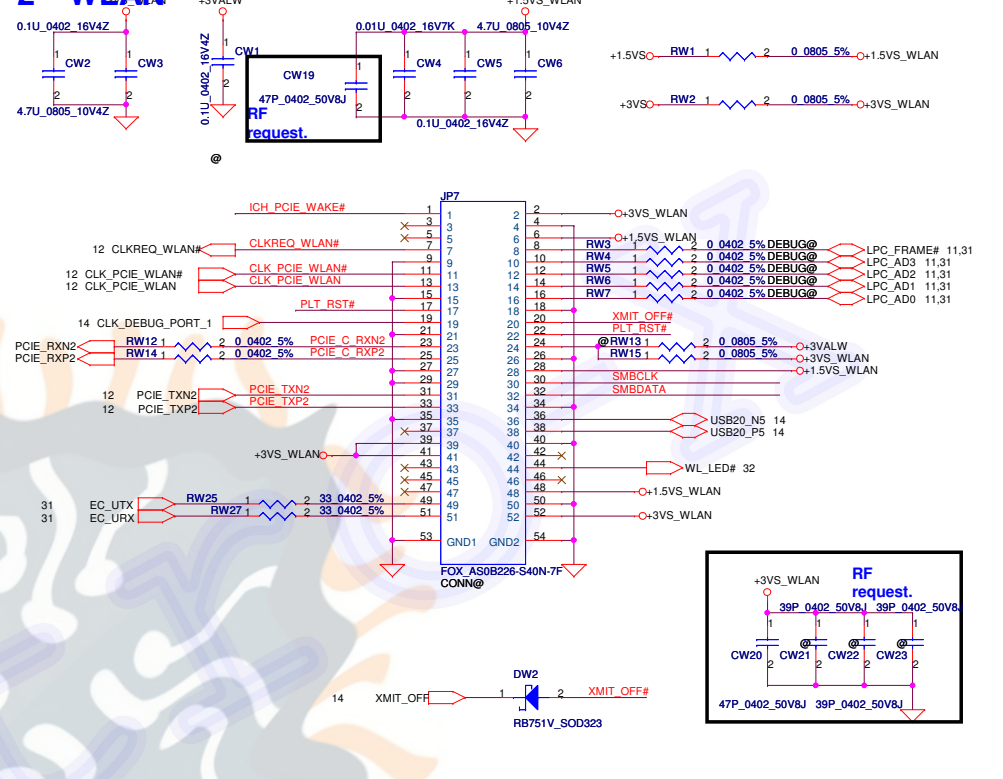


# Mini Card 0--TV tuner/WWAN/Robson

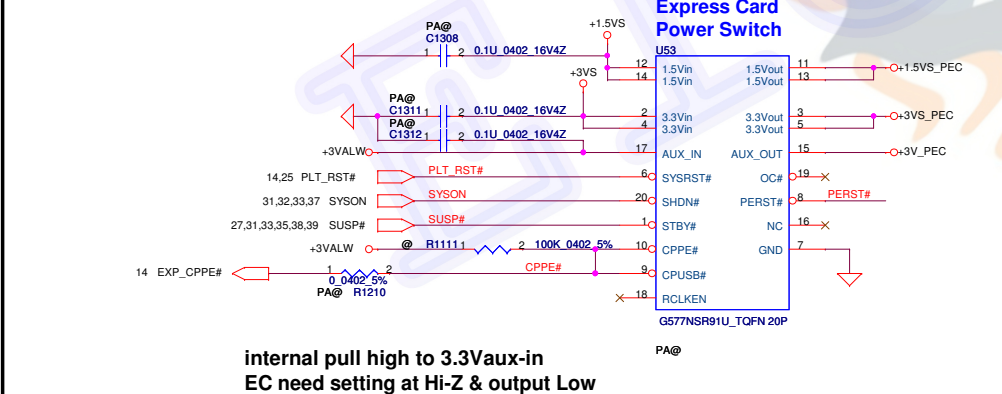
## SIM card Connector



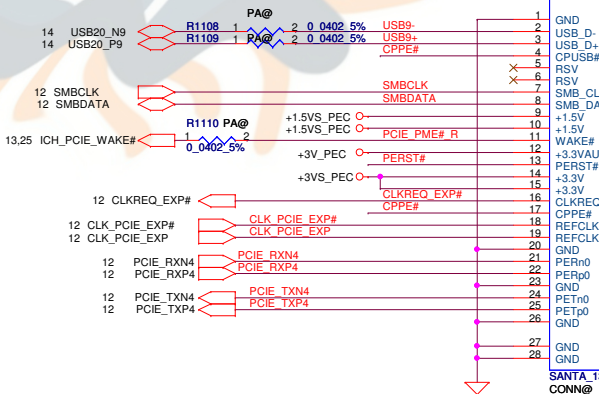
## Mini Card 2---WLAN



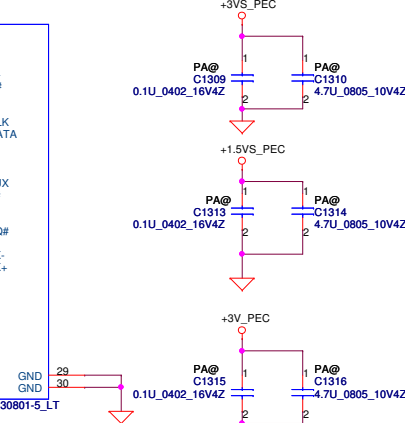
## New Card



## Close to JEXP



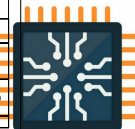
## Near to Express Card slot.



internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low

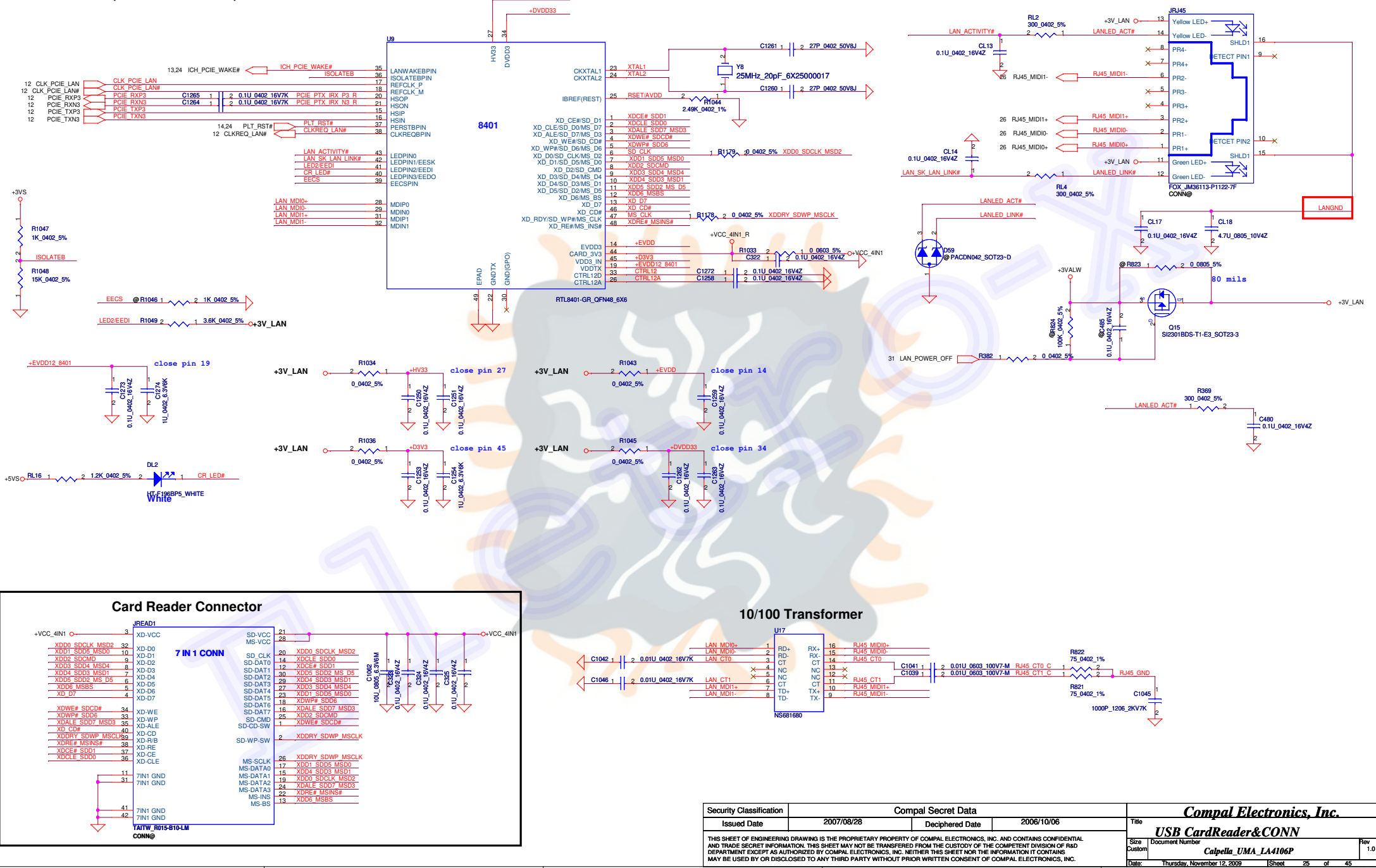
Security Classification	Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date
		2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

Title		Compal Electronics, Inc.	
WLAN, WWAN, New Card		Capella_UMA_LA4106P	
Size	Document Number	Rev	1.0
Date	Thursday, November 12, 2009	Sheet	24 of 45





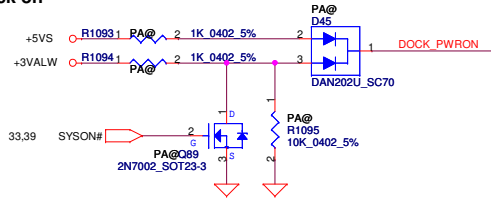
# RTL8401 Combo(LAN + Card reader)



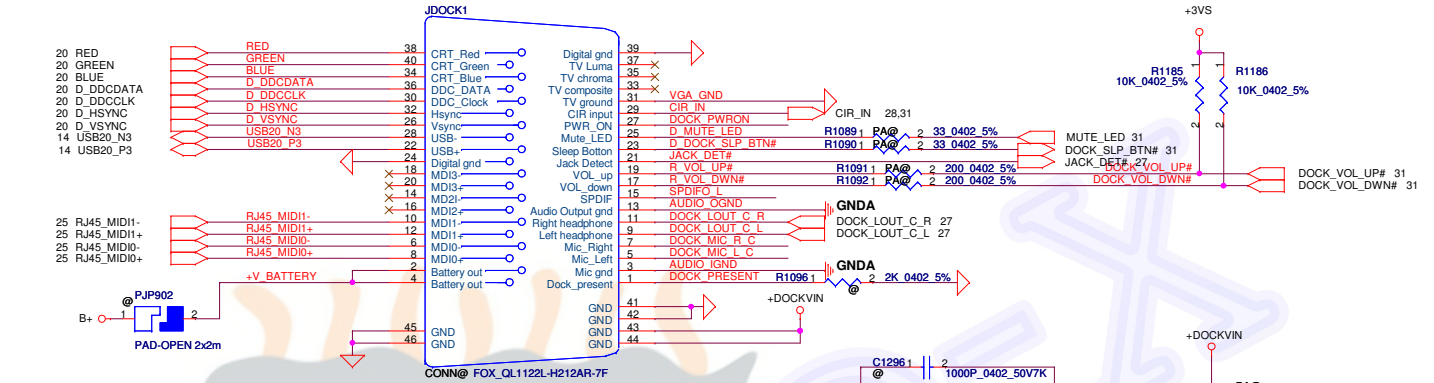
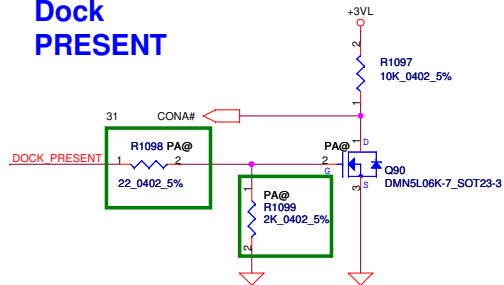


# Atlas/ Saturn Dock

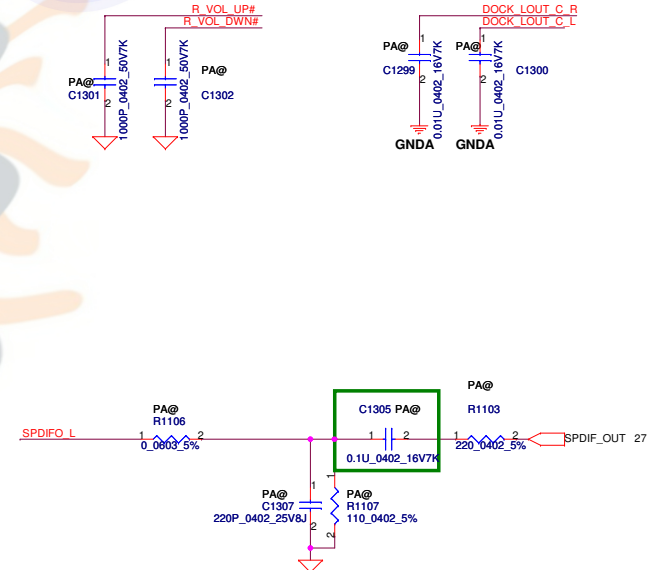
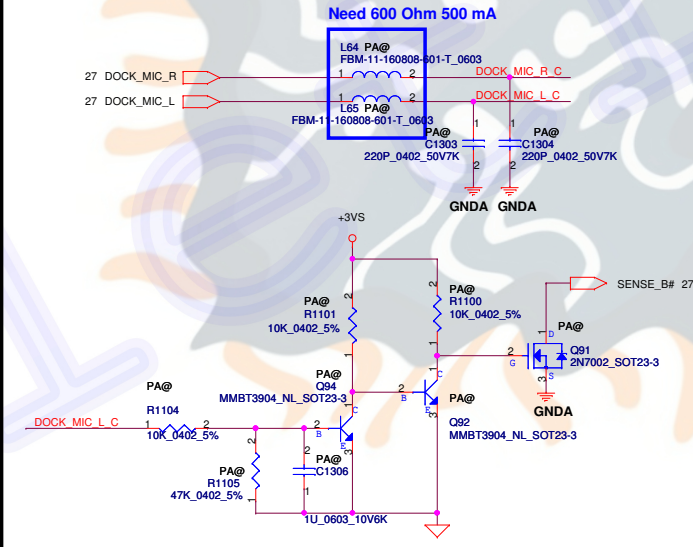
**DOCK\_PWR\_ON Spec**  
**0V** = Notebook S4/S5,  
**Dock off**  
**2.5V** = Notebook S3,  
**Dock on**  
**4V** = Notebook S0,  
**Dock on**



## Dock PRESENT



## MIC\_Dock



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	DOCK_CONN.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Customer
				Document Number	Calpella_UMA_LA4106P
				Date	Thursday, November 12, 2009
				Sheet	26 of 45
				Rev	1.0





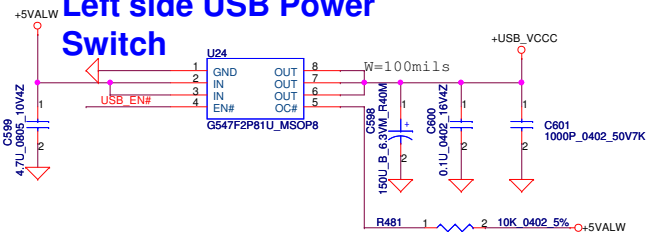




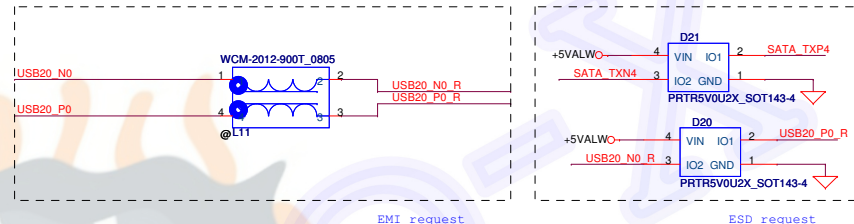
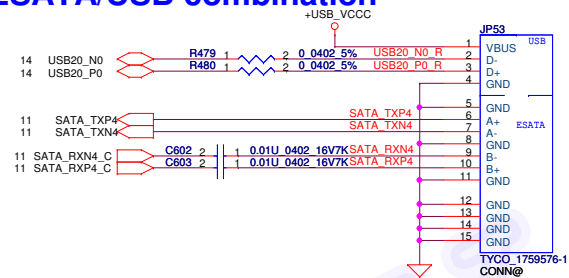




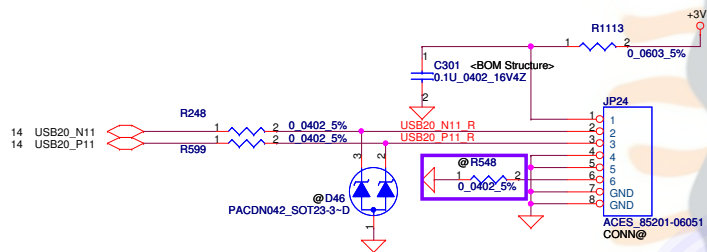
## Left side USB Power Switch



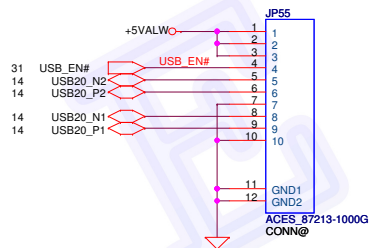
## Left\ side ESATA/USB combination Connector



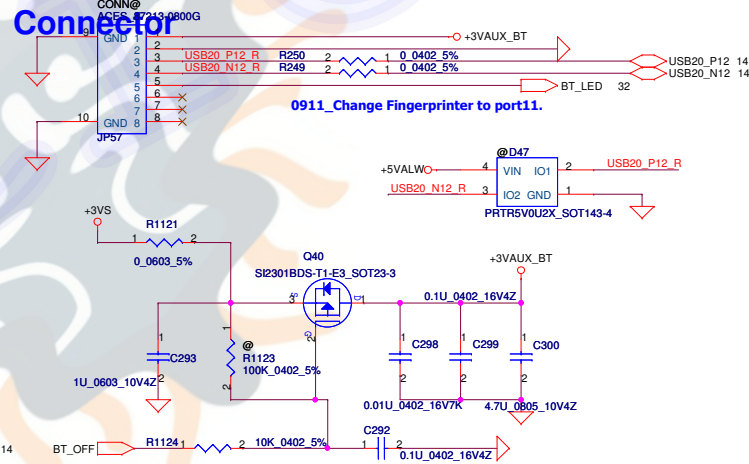
## Finger printer



## USB cable connector for Right side



## BT Connector

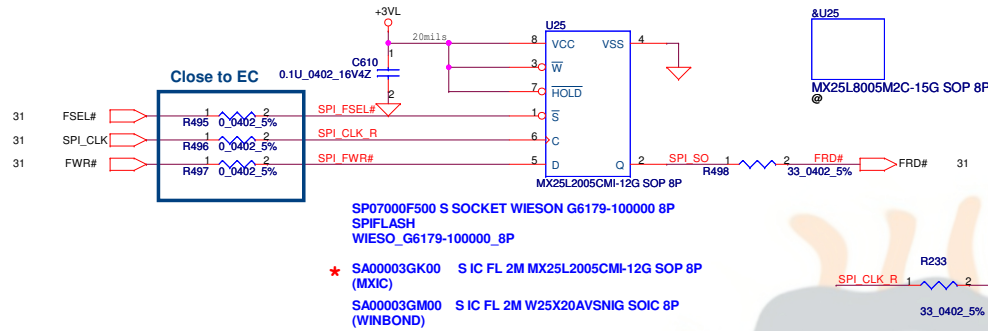


Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	USB, BT, eSATA	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Calpella_UMA_LA4106P	Rev 1.0
				Date	Thursday, November 12, 2009
				Sheet	29 of 45

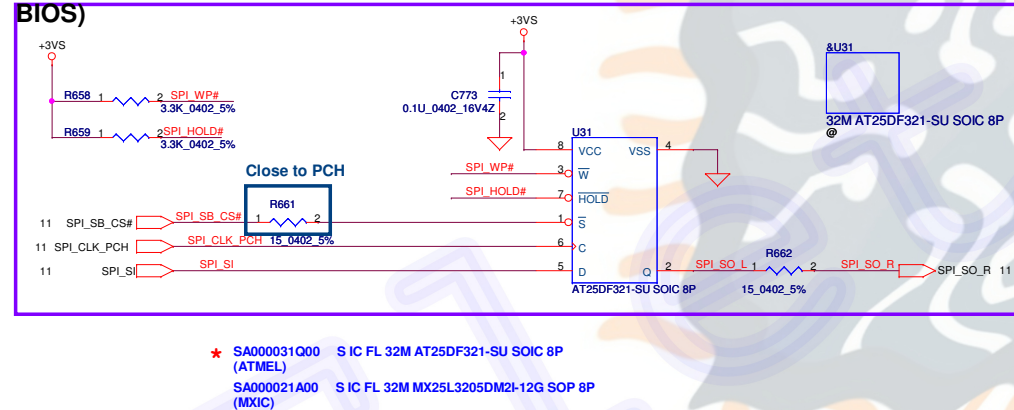




## SPI ROM => 256K (EC code)



## SPI ROM on PCH => 4M (ME code + System BIOS)



Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					Calpella_UMA_LA4106P
				Date	Thursday, November 12, 2009
				Sheet	30 of 45



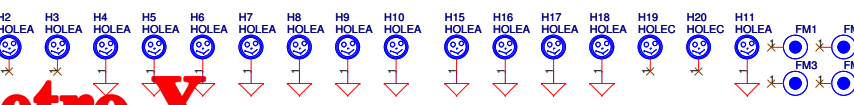
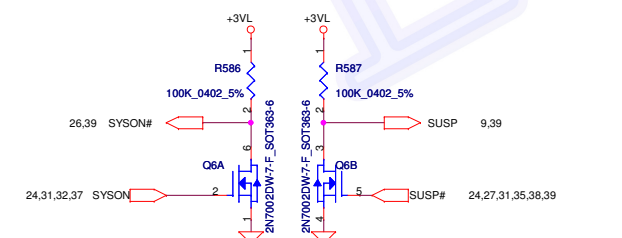
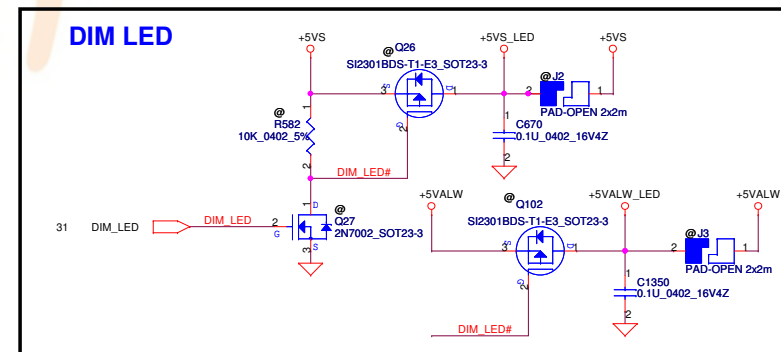
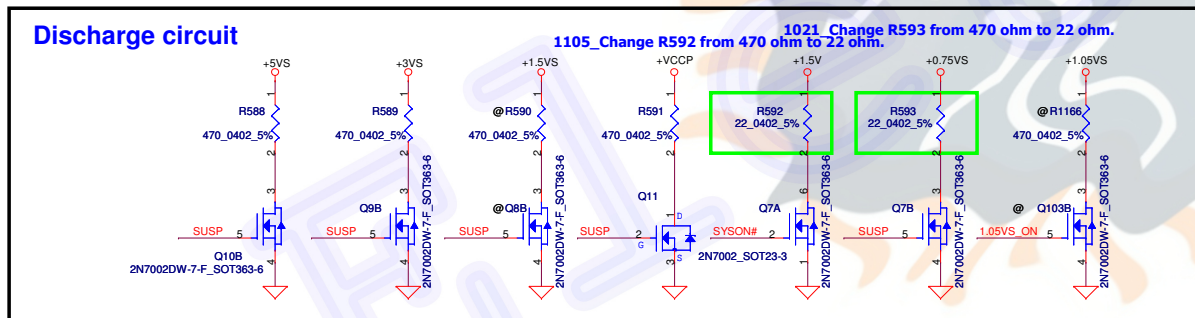
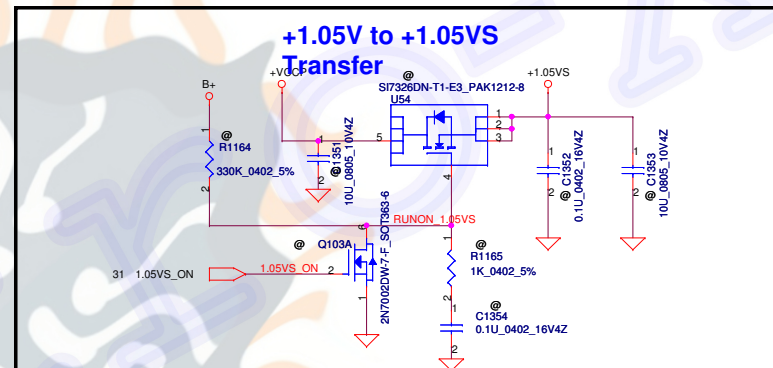
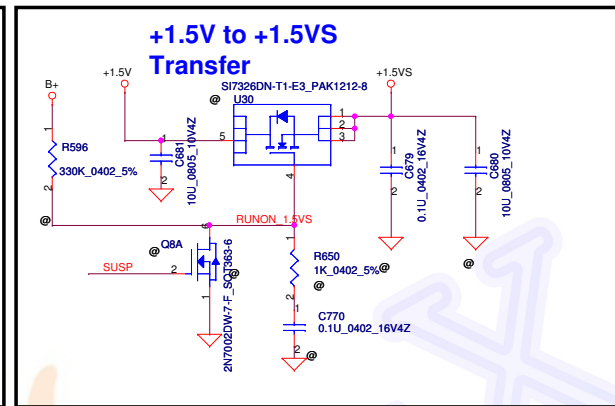
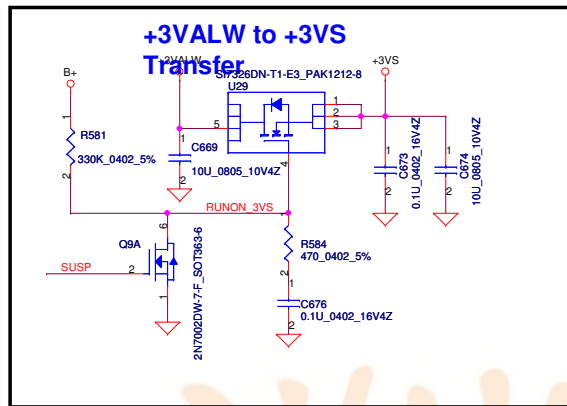
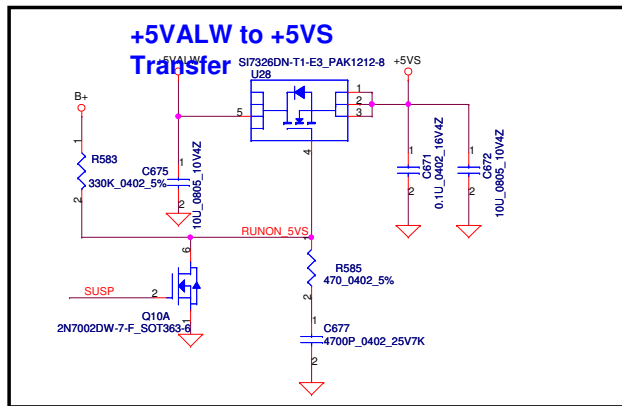






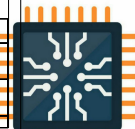




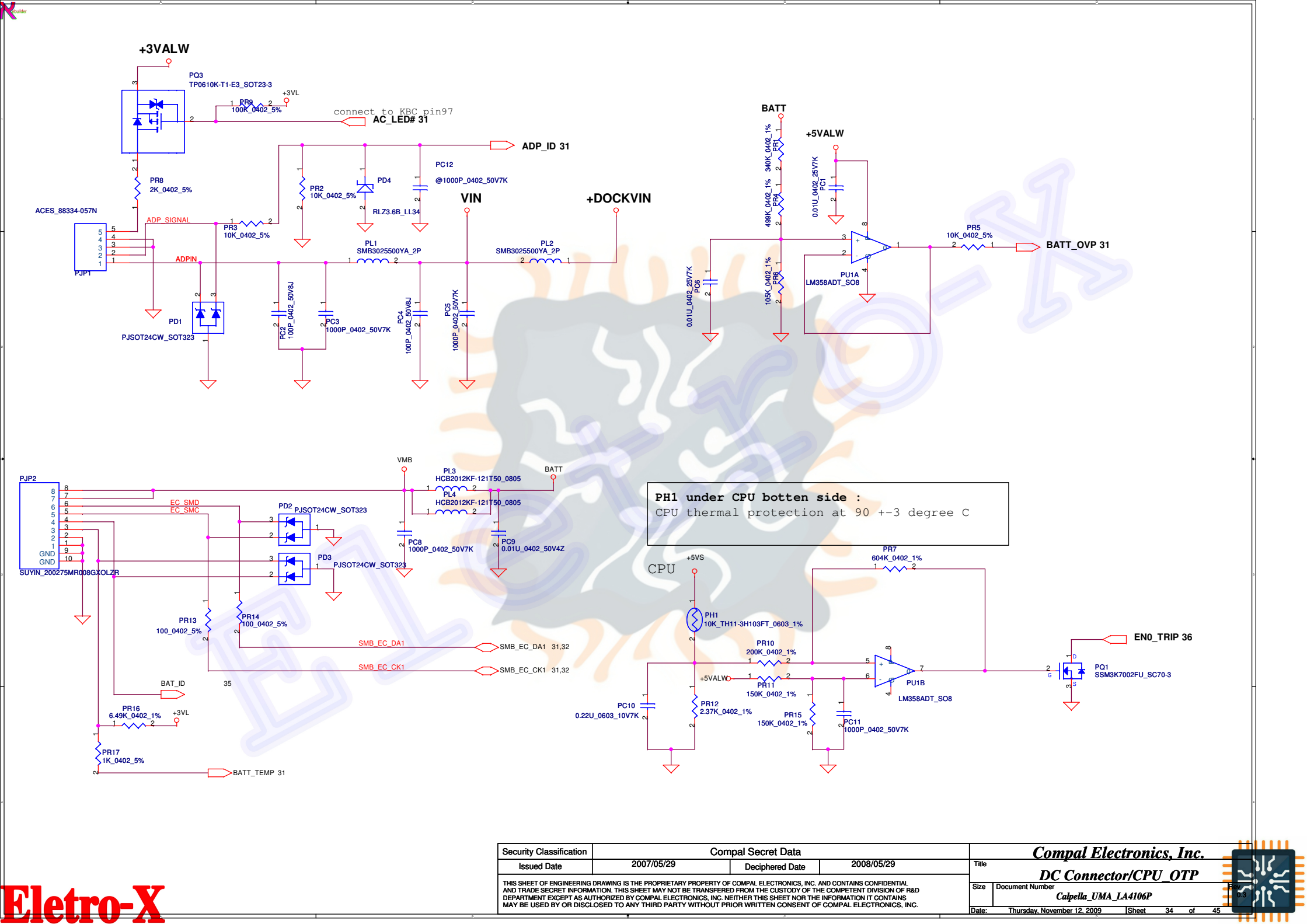


Security Classification		Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date	2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

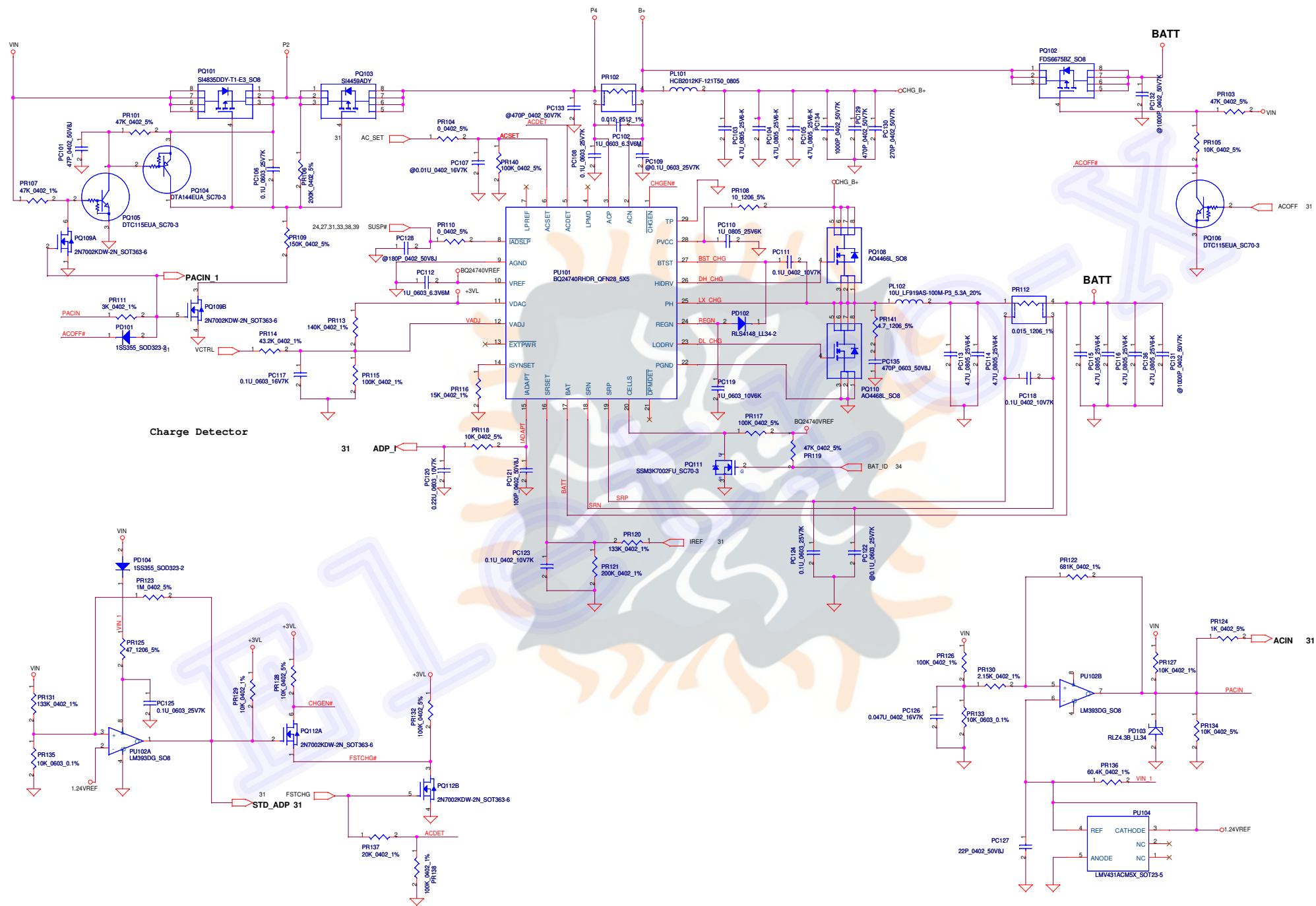
Compal Electronics, Inc.			
DC/DC Interface			
Title	Document Number	Rev	1.0
Date	Thursday, November 12, 2009	Sheet	33 of 45







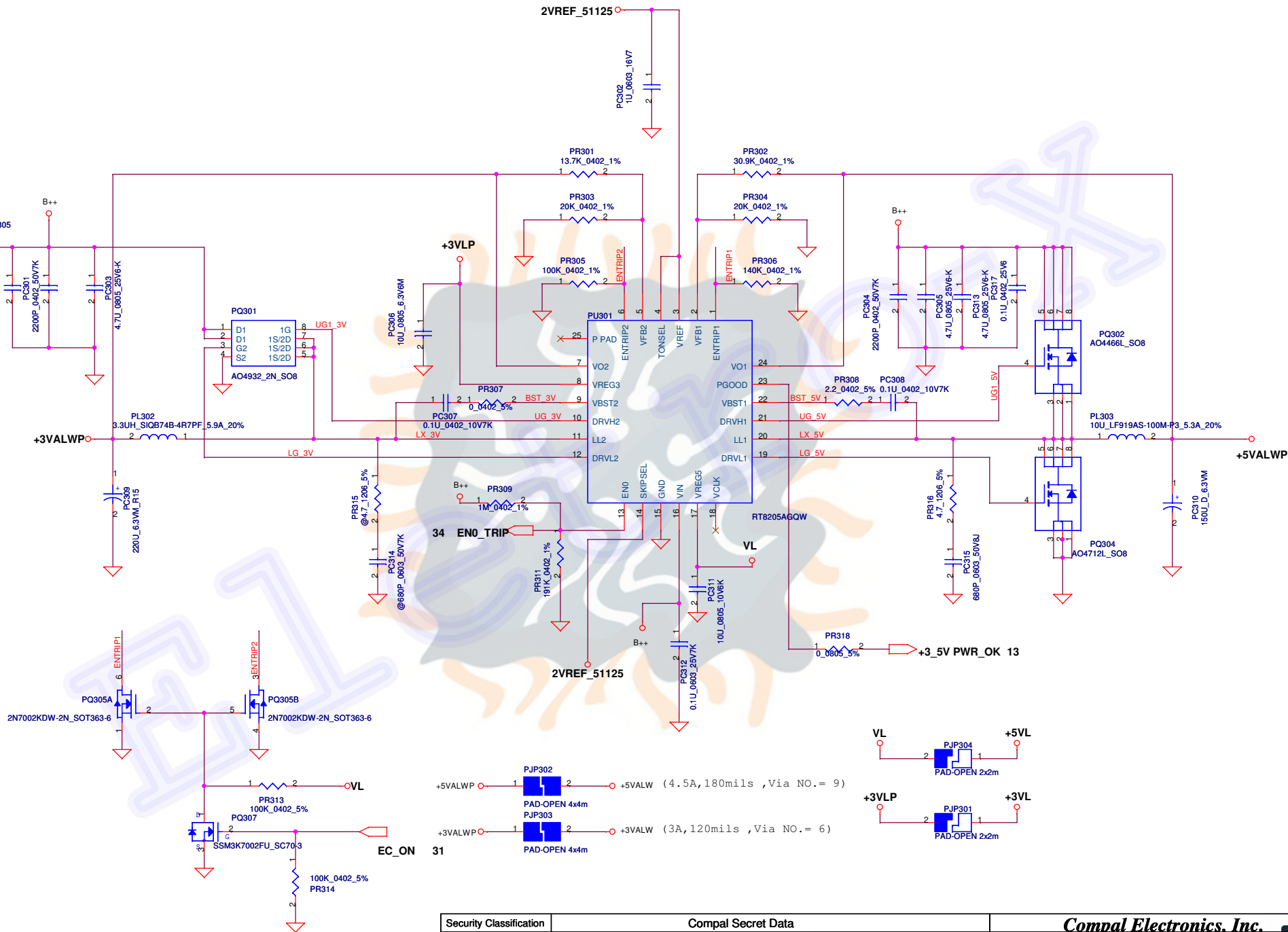




Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>Charger</b>		
Issued Date	2007/05/29	Deciphered Date	2008/05/29			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					<b>Calpella_UMA_LA4106P</b>	<b>0.3</b>
				Date:	Thursday, November 12 2009	Sheet 35 of 45





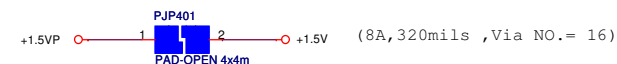
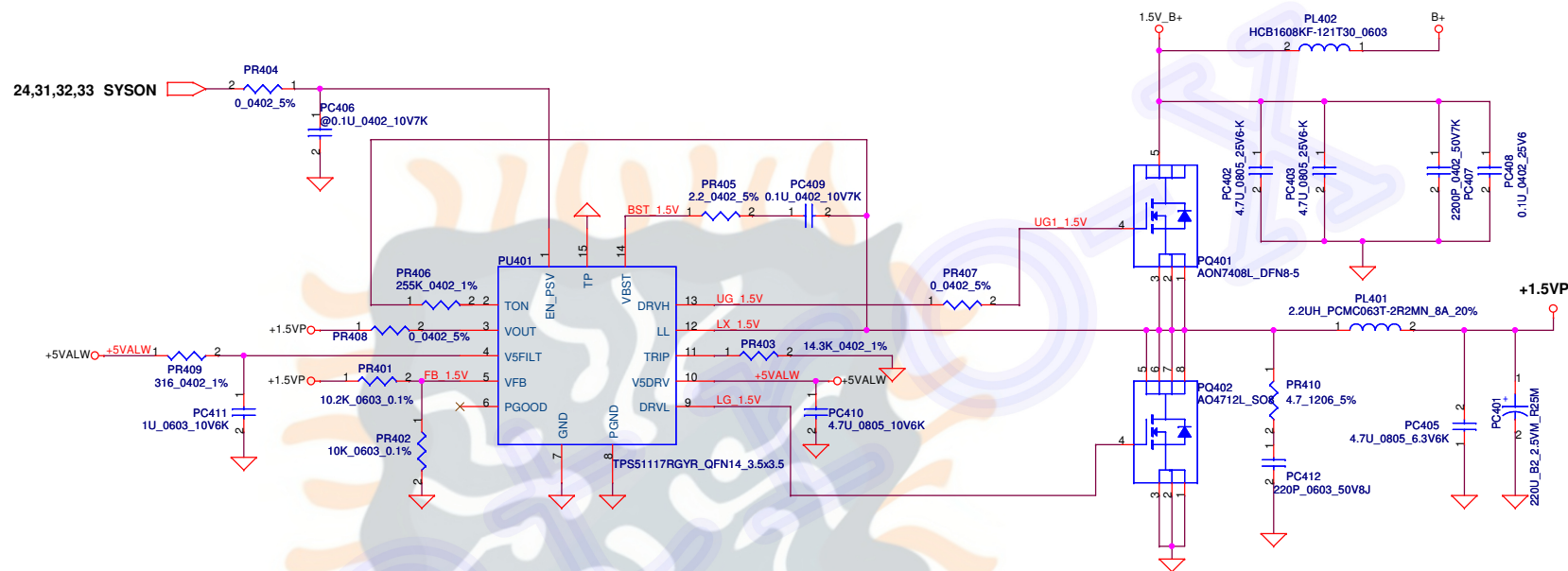


Security Classification		Compal Secret Data	
Issued Date	2007/05/29	Deciphered Date	2008/05/29
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Title	
Compal Electronics, Inc.	
3.3VALWP/5VALWP	
Size	Document Number
	Calpella_UMA_LA4106P
Date	Thursday, November 12, 2009
Sheet	36 of 45







Security Classification		Compal Secret Data	
Issued Date	2007/05/29	Deciphered Date	2008/05/29
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

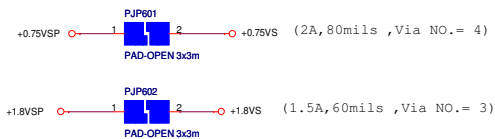
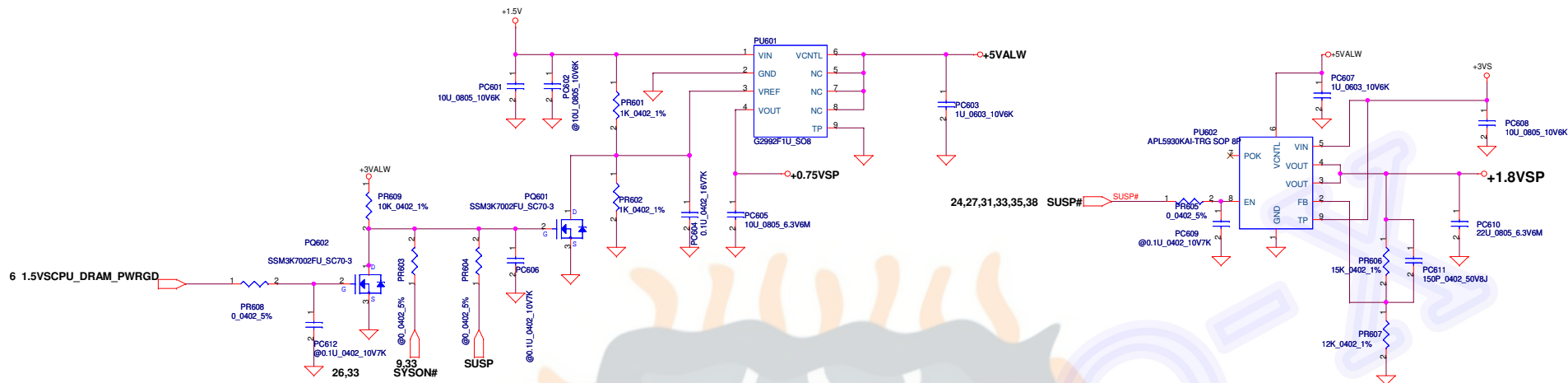
Title		Compal Electronics, Inc.	
Size		+1.5VP	
Document Number		Calpella_UMA_LA4106P	
Date:	Thursday, November 12, 2009	Sheet	37 of 45







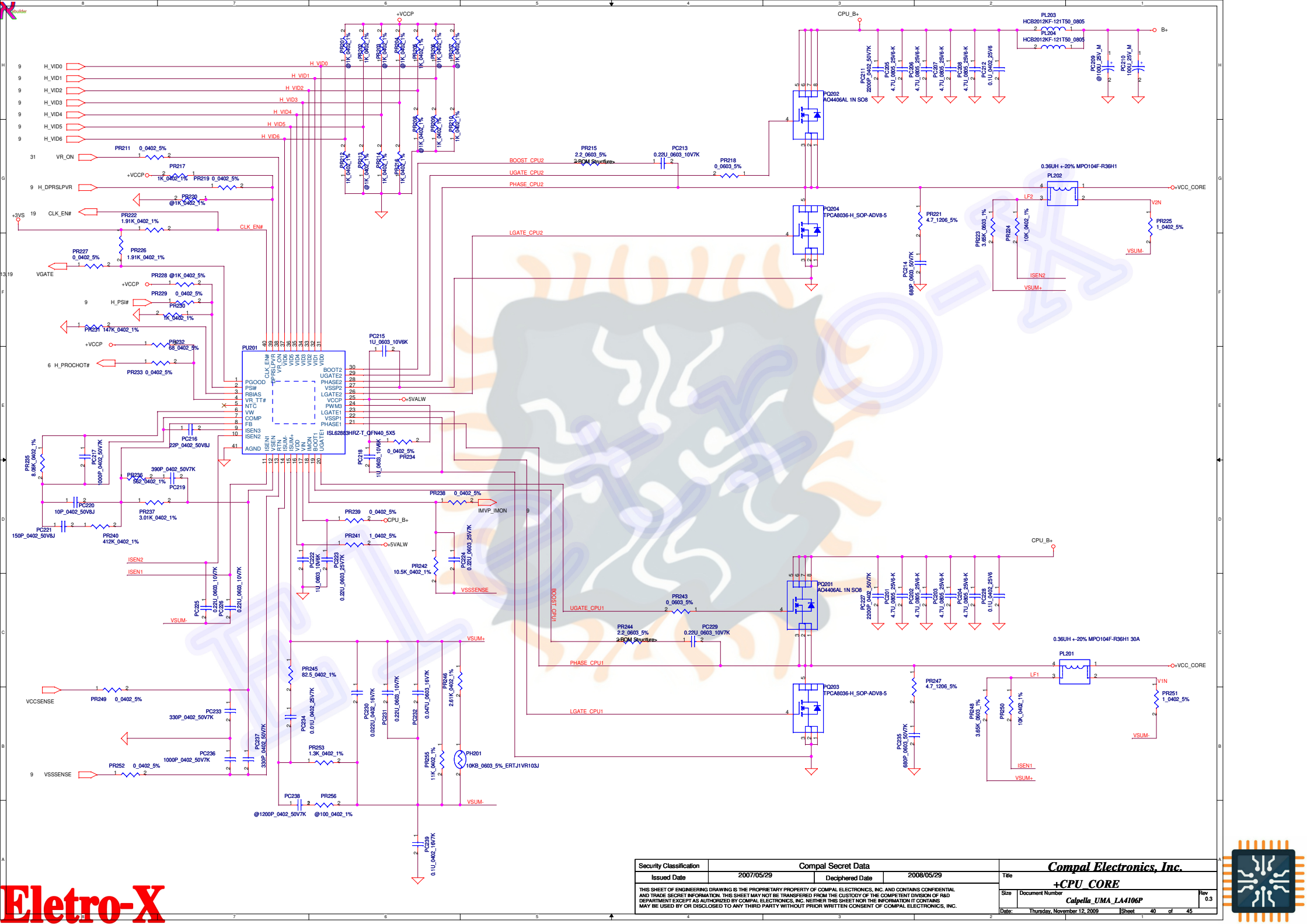




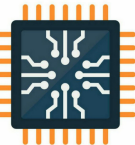
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/11/23	Deciphered Date	2007/11/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				0.75VP/1.8VSP
Size	Document Number	Calpella_UMA_LA4106P		Rev
Date	Thursday, November 12, 2009	Sheet	39 of 45	0.3



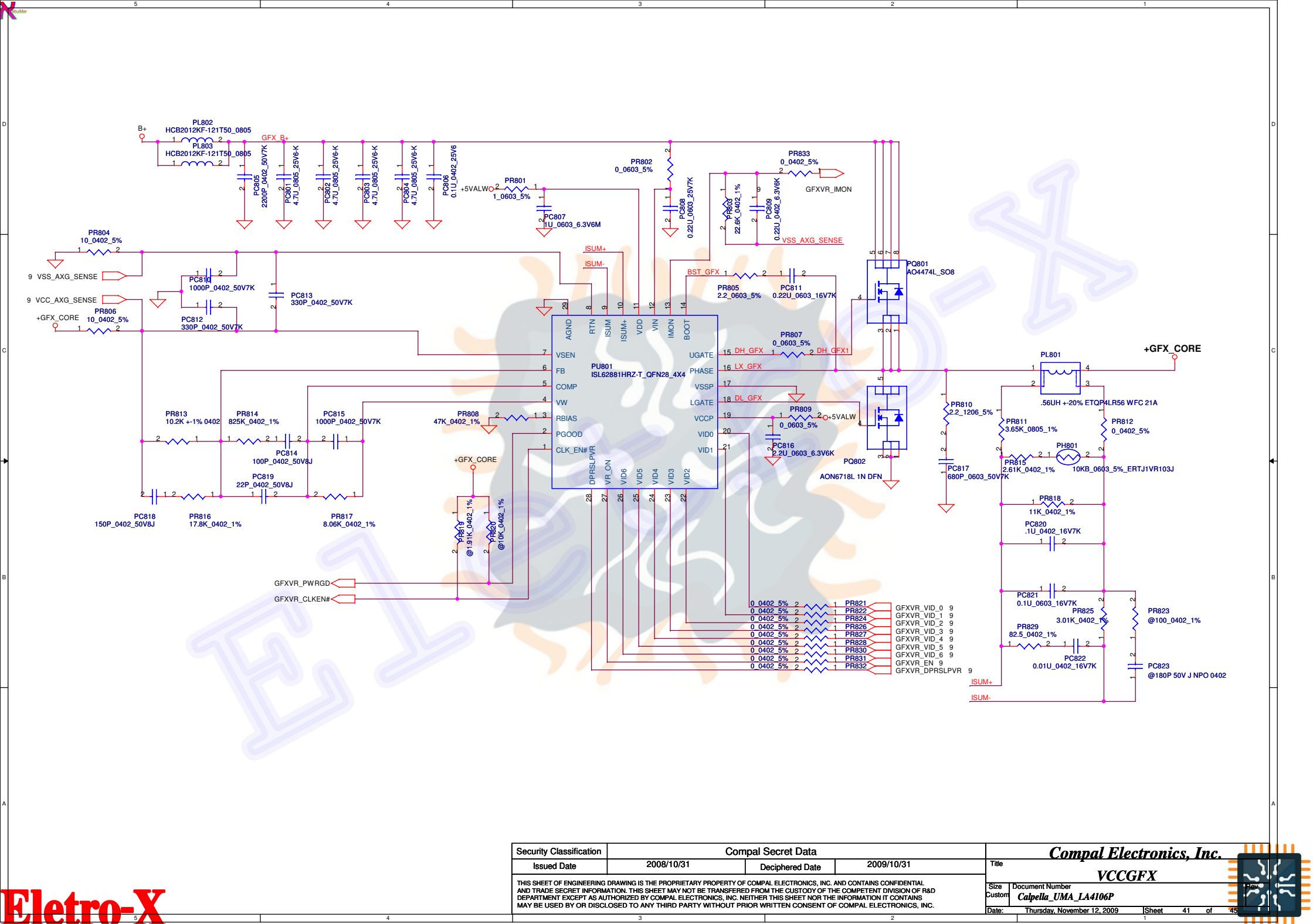




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2007/05/29		+CPU CORE	
Deciphered Date		2008/05/29		Capella_UMA_LA4106P	
Title		Size		Rev	
Document Number		40		03	
Date		Thursday, November 12, 2009		Sheet	
		40		of	
		45			







Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	Calpella_UMA_LA4106P
				Date:	Thursday, November 12, 2009
				Sheet	41 of 45



[illegible][illegible][illegible]

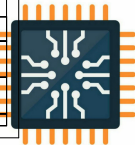


Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	22		HW	Add R801	7/20.	DB --> PV-1
02	26	Fix Volum up/down cannot work on Docking.	HW	Add R1185, R1186 and pull high to +3VS.	7/20.	DB --> PV-1
03	31	Remove double pull high resistor.	HW	Delete R660.	7/20.	DB --> PV-1
04	13	Per EMI request.	EMI	Change R679 from 33 ohm to 100 ohm.	7/20	DB --> PV-1
05	31	Modify correct pull high resistor value.	HW	Change R512 and R513 from 4.7K to 2.2K ohm.	7/20	DB --> PV-1
06	32	Modify LVDS PWM connection.	HW	Connect R890 to PCH and R505(reserve) to EC.	7/24	DB --> PV-1
07	22	Fix cannot hot plug if use Asmedia level shifter.	HW	Remove R862 and R867.	8/13	DB --> PV-1
08	22	Add series for Express card delete signal between Express card power swtich and PCH For Board ID.	HW	Add R1210	8/13	DB --> PV-1
09	31		HW	Add R386 and pull low to GND.	8/13	DB --> PV-1
10	31	Change LAN power off control pin to U27 pin115.	HW	Connect U27 pin115 and add series resistor R543 to LAN power control circuit.	8/13	DB --> PV-1
11	31	Change LID switch power rail from +3VL to +3VALW.	HW	Pull high R526 to +3VALW.	8/13	DB --> PV-1
12	31	Delete useless parts.	HW	Delete R542 because already connect EC_UTX to MINI PCIE connector	8/13	DB --> PV-1
13	32	Change LID switch power rail from +3VL to +3VALW.	HW	Change JP11 pin 1 to +3VLALW.	8/13	DB --> PV-1
14	33	For Cost down.	HW	Reserve U30, R596, R650, R590, C681, C770, C679, C680, Q8; add PJ2 to connect +1.5VS_CPU and +1.5VS power plan.	8/13	DB --> PV-1
15	33	Try to use +1.5VS to replace +1.8VS power rail.	HW	Add and reserve PJ3 to short +1.8VS and +1.5VS_CPU power plan.	8/13	DB --> PV-1
16	14	Modify prevent S3 leakage issue circuit.	HW	Connect PCH_DDR_RST from EC GPIO48 to PCH GPIO46.	8/13	DB --> PV-1
17	31	Modify prevent S3 leakage issue circuit.	HW	Delete R386	8/13	DB --> PV-1
18	21	Fix LCD panel no display issue.	HW	Connect JLVDS1 pin27 to +3VS.	8/13	DB --> PV-1
19	32	Change Cap. board power rail from +3VL to +3VS.	HW	Reserve R1211 and connect to +3VS.	8/13	DB --> PV-1
20	27	Swap Audio port A and F.	HW	Swap port A and port F. Detail please see audio circuit.	8/17	DB --> PV-1
21	6	Delete XDP connector	HW	Delete JP1, R13, R17, R18, R19, R22, R25, C1	8/17	DB --> PV-1
22	25	Conecto Q15 to +3V_LAN.	HW	Delete R1031 and connect Q15 pin1 to +3V_LAN directly.	8/17	DB --> PV-1
23	26	Modify Audio circuit near docking side.	HW	Connect Q91 pin3 to GNDA and move it near Codec.	8/17	DB --> PV-1
24	27	Per EMI/ESD request.	EMI/ESD	Add R1212/C1433 for HDA_RST#_CODEC. Add C1434. Change R132/R135/R139 to C1435/C1436/C1437.	8/17	DB --> PV-1
25	6	Modify prevent S3 leakage issue circuit.	HW	Change U57 from reset IC to AND gate; add R1218 and reserve R383; add voltage divider(R1216/R1217) for VITPWGOOD.	8/19	DB --> PV-1
26	25	Follow DIS.	HW	Change Y8 material.	8/19	DB --> PV-1
27	28	Per ESD request.	ESD	Add D61, D62 for OPP sku.	8/19	DB --> PV-1
28	32	Change cap. board power rail from +3VL to +3VS.	HW	Pull high R544 and R545 to +3VS power rail.	8/20	DB --> PV-1
29	14	Make sure PLT_RST# level is stable.	HW	Stuff R185.	8/20	DB --> PV-1
30	32	Reserve +3VL power rail for cap. board.	HW	Add and reserve R1219/R1220 to +3VL.	8/21	DB --> PV-1





Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	6	Make sure +1.5VS can ramp up early than +0.75VS.	HW	Connect 1.5VSCPU_DRAM_PWRGD to enable PU601.	9/11	PV-1 --> PV-2
02	11	ME fuction control enable/disable.	SW/EC	Add Q106, R1221, R1222 and connect to EC pin26.	9/11	PV-1 --> PV-2
03	13	For support ME function.	SW/EC	Connect SUS_PWR_ACK to EC pin76.	9/11	PV-1 --> PV-2
04	14	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
05	27	To solve no Vref out when external MIC change from port A to port F.	HW	Reserve R431, add R and connect to +AVDD_CODEC.	9/11	PV-1 --> PV-2
06	27	Delete EC_BEEP from EC because useless.	HW	Delete EC_BEEP to EC.		
07	28	Delete ANA_MIC_DET net to EC.because useless.	HW	Delete ANA_MIC_DET to EC.	9/11	PV-1 --> PV-2
08	29	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
09	31	Board ID is not enough when use pin81.	EC	Swap TP_BTN# and BDID, then add pull high resistor R1223 for BDID.	9/11	PV-1 --> PV-2
10	31	ME fuction control enable/disable.	SW/EC	Remove EC_BEEP and change to ME_EN, then connect ME_EN to Q106.	9/11	PV-1 --> PV-2
11	31	For support ME function.	SW/EC	Remove ANA_MIC_DET and change to SUS_PWR_ACK, then connect SUS_PWR_ACK to PCH.	9/11	PV-1 --> PV-2
12	31	Chagne ENE cap. board ESB bus power rail from +3VS to +3VL.	HW	Reserve R544/R545 and stuff R1219/R1220.	9/11	PV-1 --> PV-2
13	32	Chagnge Cap. board power rail from +3VS to +3VL.	HW	Reserve R1211 and stuff R1140.	9/11	PV-1 --> PV-2
14					9/11	PV-1 --> PV-2





Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	12	To solve RTL8401 cause BSOD 0xD1 issue.	HW	Change RTL8401 PCIE port from port3 to port5 (follow Rhett2.0), new add series resistor R506/0 ohm.	10/19	Delete this item in 10/26.
02	12	To solve HDMI signal jitter fail issue.	Intel	Add Y2, R131, C141. Change C142 from 0 ohm to 18pF.	10/19	PV-2 --> MV
03	19	To solve time too fast in DOS mode.	HW	Change R259 and R260 from 18pF to 22pF.	10/19	PV-2 --> MV
04	25	To solve RTL8401 cause BSOD 0xD1 issue.	HW	Change RTL8401 PCIE port from port3 to port5 (follow Rhett2.0)	10/19	Delete this item in 10/26.
05	31	To solve cannot power on when no CPU insert in ATE test.	HW	Add pull high resistro R13 to +3VL_EC for EC pin21.	10/20	PV-2 --> MV
06	33	To meet Intel power down sequence spec.	HW	Change R593 from 470 ohm to 22 ohm.	10/21	PV-2 --> MV
07	09	To meet Intel power down sequence spec.	HW	Change R1182 from 470 ohm to 220 ohm.	10/21	PV-2 --> MV
08	13	Follow Intel schematic checklist rev2.0 change.	HW	Change R137 from 1K ohm to 10K ohm.	10/21	PV-2 --> MV
09	27	To solve audio noise issue.	HW	Add and reserve U59, R1228, C1443, C1444, C1445, C1446, R1226, R1227.	11/02	PV-2 --> MV
10	04	To solve ESD test fail.	ESD	Add and reserve C1438, C1439, C1440 near Q104.	11/03	PV-2 --> MV
11	17	To solve ESD test fail.	ESD	Add and reserve C1441 near JDIMM1.	11/03	PV-2 --> MV
12	18	To solve ESD test fail.	ESD	Add and reserve C1442 near JDIMM2.	11/03	PV-2 --> MV
13	28	To solve ESD test fail.	ESD	Add and reserve C1447 between GND and GNDA near internal MIC connector.	11/03	PV-2 --> MV
14	32	To solve EMI test fail.	EMI	Change R1148 from 0 ohm to bead (SM01000CY00), move C652 to near JP59.	11/03	PV-2 --> MV
15	32	To solve EMI test fail.	EMI	Move C652 to near JP59.	11/03	PV-2 --> MV
16	27	To solve audio noise issue.	EMI	Move C652 to near JP59.	11/03	PV-2 --> MV
17	27	Reserve ref. power for external MIC.	HW	Reserve R1230 to connect +VREFOUT_INMIC.	11/05	PV-2 --> MV
18	27	To solve GFX power spike when S0 to S3/S5.	Intel	Change R43 from 4.7K ohm to 249 ohm.	11/05	PV-2 --> MV
19	33	To meet Intel power down sequence spec.	HW	Change R592 from 470 ohm to 22 ohm.	11/05	PV-2 --> MV
20	6	To reduce powr noise from FAN.	HW	Add R597.	11/05	PV-2 --> MV

